NELC / TR 2020

NELC / TR 2020

ADA039962

(12)

SECOND ANNUAL REPORT
ADVANCED MAIL SYSTEMS SCANNER TECHNOLOGY

Volume 1: Executive Summary and Appendixes A-F

October 1976

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FOR THE
US POSTAL SERVICE
OFFICE OF ADVANCED MAIL SYSTEMS DEVELOPMENT

AMSD

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SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER
NELC Technical Report 2020 (TR 2020)

2. GOVT ACCESSION NO.

3. ~~RECIPIENT'S CATALOG NUMBER~~
(14) NELC/TR-2020-Vol-1

4. ~~TITLE (and Subtitle)~~
(6) ADVANCED MAIL SYSTEMS SCANNER TECHNOLOGY.
~~Second Annual Report~~
Volume 1. Executive Summary and Appendixes A-F.
(9) Annual rept. no. 2, 10 Oct 75 - 9 Oct 76.

5. TYPE OF REPORT & PERIOD COVERED
Annual, 10 October 1975 to 9 October 1976

6. PERFORMING ORG. REPORT NUMBER

7. AUTHOR(s)
NELC ~~Display Division (Code 3100)~~
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8. CONTRACT OR GRANT NUMBER(s)
Agreement 104230-76-T-0798

9. PERFORMING ORGANIZATION NAME AND ADDRESS
Naval Electronics Laboratory Center
San Diego, California 92152

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
O, USPS, O (NELC N451)

11. CONTROLLING OFFICE NAME AND ADDRESS
Office of Advanced Mail Systems Development
US Postal Service, 1171 Parklawn Ave., Rockville, MD 20852
Attn: Mr VP Boyd, Program Manager

12. REPORT DATE
(11) October 1976

13. NUMBER OF PAGES
358
(12) 359p.

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)

15. SECURITY CLASS. (of this report)
UNCLASSIFIED

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)
Approved for public release, distribution is unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

403 940

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Charge coupled devices	Image storage	Self-scanned arrays
Data compression	Optical scanning	Solid-state scanners
Image acquisition	Photodiodes	Video processing
Image processing	Run length coding	

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objective of the effort described herein is to provide technical consultation, equipment, and support services to the US Postal Service which will contribute to the development of the system definition of a new-concept processing system, the Electronic Message Service (EMS). Included in the scope of effort are investigations of high-speed image scanning technology, image frame memory storage, image enhancement, and the fabrication of a scanner/frame store memory test assembly.

This is Volume 1 of the second annual report. Volume 2 contains proprietary information and is available to Government agencies only.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE
S/N 0102-LF-014-6601

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The citation of trade names and names of manufacturers in this report is not to be construed as official Government indorsement or approval of commercial products or services referenced herein.

OBJECTIVES

1. Provide the US Postal Service the technical consultation, equipment, and support services which will contribute to the development of the system definition of a new-concept processing system, the Electronic Message Service (EMS). Include in the scope of effort (1) investigations in scanner technology, image frame memory storage, and image enhancement, and (2) the design and fabrication of a scanner/frame store memory test assembly.

2. Contribute to the selection of the most optimum imaging devices and techniques for high-speed image acquisition. Provide reliable designs of high-speed image processing logic which will preserve the quality of the image while reducing the image storage and transmission requirements and minimizing vulnerability of the image information to noise during processing, transmission, and reproduction.

3. Act as technical consultants to the USPS Office of Advanced Mail Systems Development in preparing technical requirements and statements of work and evaluating technical proposals and contractor performance; and perform technical evaluation of contractor-produced developmental equipment.

RESULTS

1. A large drum test bed (LDTB) was designed and fabricated, compatible with Pitney Bowes paper handling equipment.

2. High-brightness fluorescent lamps were evaluated for use in the LDTB and found to be superior, for this application, to the quartz halogen lamp used in the small drum test bed that was developed during the previous year.

3. Software was developed to compensate for nonuniform illumination.

4. Special fluorescent lamps were procured in which the mixture of phosphors compensates for falloff in imager sensitivity from red to blue.

5. Test and evaluation of imagers continued. The ranking of the contenders changed as the result of the emergence of new and improved devices.

6. New CCD driver boards incorporating best available high-speed logic techniques were designed and fabricated.

7. Image analyzer capability was expanded so that first derivative and run length statistics may be provided in addition to the original pel brightness statistics.

8. Progress was recorded throughout the software hierarchy running from microcodes up to high-level procedural programs. Corresponding hardware improvements were effected. High-speed PROMs incorporating microcode data, for example, replaced the low-speed PROMs previously used in the memory controller.

9. Six technical reports were submitted to AMSD in the reporting period. They are included here as appendixes.

10. A contract was issued to RCA Princeton for the development of a tracking/time-delay-integration imager.

PLANNED FUTURE NELC ACTIVITIES

1. Evaluate new imagers that may be suitable for EMS.

2. Continue hardware and software investigative efforts in the areas of buffers, coding, compression, enhancement, processing, and analysis.

3. Evaluate techniques for recreating stored images.

ADMINISTRATIVE INFORMATION

This report contains a summary of work sponsored by the Office of Advanced Mail Systems Development, Planning and New Development Department of the US Postal Service, Rockville, Maryland 20852, under USPS/NELC Agreement 104230-76-T-0798. The contractual period was 10 October 1975 to 9 October 1976. The authorized USPS technical representative is Victor P Boyd. The principal investigator is Frank C Martin of the Display Division, NELC Code 3160. Associate investigators are Waldo Robinson, Tom Little, Lee Wise, Joseph Greene, Clint Mayo, and Bob Basinger, all of Code 3160. This report is a compilation of data presented by all team members and was approved for publication October 1976.

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GLOSSARY

GLOSSARY

A/D	Analog to digital
ALRU	Arithmetic logic register unit
ALU	Arithmetic logic unit
AMSD	Office of Advanced Mail System Development
CCD	Charge-coupled device
CPE	Central processing element
CRT	Cathode ray tube
D/A	Digital to analog
DIA	Digital image analyzer
EAROM	Electrically alterable read only memory
ECL	Emitter coupled logic
EMS	Electronic Message Service
FD stats	First derivative statistics
Frame store memory	The 3×10^6 bit memory used for storing imager data prior to processing and image storage for anything displayed on the high-resolution monitor
FSMC	Frame store memory controller, the primary control electronics for the test bed
GFE	Government-furnished equipment
I^2L	Integrated injection logic
Image analyzer	A module of electronics circuitry that generates the FD, PB, or RL statistics according to wired programs
LDTB	Large drum test bed, which includes the 40-inch circumference drum, drive motors, illumination sources, imager, imaging lens, imager driver board, analog-to digital converter, and power supplies
LED	Light emitting diode
LSB	Least significant bit
LSI	Large scale integration
MARB	Memory address register bus
MOS	Metal oxide semiconductor
MTBF	Mean time between failures
NELC	Naval Electronics Laboratory Center
PB stats	Pel brightness statistics
Pel	One photosensitive element of an imaging device
PROM	Programmable read-only memory
RAM	Random access memory
RL stats	Run length statistics

ROM	Read only memory
SDB	Secondary data bus
SDTB	Small drum test bed, which includes same as LDTB except for size of drum, which has 12-inch circumference
TDI	Time delay integration
Test bed	The entire complement of hardware being developed by NELC for USPS
TTL	Transistor-transistor logic
USPS	United States Postal Service
VTS	Video Transmission System (Navy)
"WEBERVERT"	Convert from linear amplitude steps to geometrically proportional steps, similar to but in larger ratios than Weber's fraction

RELEVANCE TO DoD MISSION

RELEVANCE TO DoD MISSION

If instrumented, the Electronic Message Service (EMS) system will become the second-largest communication and information exchange system in the US. Participation on the imaging interface aspects of the system provides familiarity for our Navy group, who will be able to assist in utilization of the network for military purposes in a time of national need.

The actual imaging investigation is relevant to recent and current NELC programs such as DCA facsimile by Codes 1400 and 3500, the Electro-Optical Submarine Mast by Code 2500, and the facsimile programs of Code 3200.* One of the requirements of the Tactical Flag Command Center program is image transmission. Other requirements for image acquisition, processing, and transmission are implicated in work for the Naval Intelligence Support Center. The USPS test bed has been designed to interchange data with the NELC video test bed in Code 3140.

One of the program procurements is a large, high-speed imaging, charge-coupled device (CCD) which can operate in the time-delay integration (TDI) mode. This single device is capable of acquiring full-page data at a rate of 20 pages per second. The high performance of the device makes it applicable for telereconnaissance, teleguidance, battlefield surveillance, and intrusion detection as well as document imaging.

The experience gained with microprocessor architecture, image processing, high-speed storage and retrieval, display, and hard-copy generation is also valuable to the Navy. There does not appear to be much image processing capability within DoD activities (outside the intelligence community). ARPA and others are supporting universities which are doing excellent image processing studies in software programs on general-purpose computers. Very little of the work addresses the high-speed, real-time hardware and algorithm requirements of military applications.

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*NELC Code 1400	=	Satellite Systems Program Office
3500	=	Internal Communications and Tech Control Division
2500	=	EO/Optics Division
3200	=	Communications Processing Division

EXECUTIVE SUMMARY

EMS BACKGROUND

Mail has long been a material concept. A "piece" of mail is a tangible document, in an envelope, with another material thing, a stamp, pasted on the envelope. Mail is "posted" – dropped into a box. It is "picked up," "carried" by truck, train, or plane, and ultimately "delivered."

Mail of this familiar variety is so common that in the US alone billions of letters are delivered every year, and the number is growing. The load is monumental, and fleets of planes and other vehicles and armies of mailmen are hard pressed to handle it. Demand for reliable service and rapid delivery adds a dimension to the problem.

But mail has another aspect which is not physical. Mail is intelligence, and obviously the job of moving the mail from one city to another will be significantly lightened when it can be reduced to moving the message, divested of paper, envelope, and stamp.

With this objective, the USPS has undertaken the investigation of advanced mail systems. An important element in this program is the investigation of a possible Electronic Message Service (EMS). The USPS is conducting a detailed system definition effort for the purpose of establishing the technical and economic feasibility of a nationwide EMS concept. The attractive economics of available wideband telecommunications systems strongly suggest that the USPS should look at such large-scale message systems as a new means of providing basic message services at reduced costs to the USPS customer.

Functionally, EMS would accept messages in digital or paper copy form, convert inputs, as required, into digital form, transport message inputs electronically from source to EMS destination over communication networks, and either convert the message back to paper copy form for carrier delivery to the recipient or deliver it to the customer by alternative electronic delivery systems.

The USPS is investigating EMS because it has the potential capability of coping with anticipated changes in mail volume and mail patterns, and of taking advantage of the expanding utilization of electronic technology within the business world. It is anticipated that EMS will provide the customer with a faster, more reliable, low-cost service and that it will contribute to balancing postal costs and revenues as required by the Postal Reorganization Act.

EMS CONCEPTS

To provide this better service, the Electronic Message Service envisioned by the Postal Service would be set up as a national system capable of processing a tremendous volume of messages, mostly business-oriented. Targeted as a possible replacement for first class mail and a partial alternative to third class, the system would be a complex network made up of user terminals, stations, and centers (see figure 1).

The EMS centers would interconnect the net links, performing data storing and switching tasks. The EMS stations, set up at regional post offices or branches, would contain terminals and an assortment of conversion gear – OCR (optical character recognition), microfiche readers, magnetic tape devices, and scanners to read the computer messages.

A customer will go to the nearest terminal to "post" a letter. The message input will be converted to compatible digital form and transmitted electronically to its destination, probably through a mixed hybrid terrestrial satellite network. At its destination, the message will be either changed back to paper copy form for hand delivery by the postman, or delivered electronically.

It is evident that a critical area of technology, for a successful EMS, is the ability to accept and convert a customer message with a very high degree of accuracy across a broad range of input documents. A system with limited input range or very restrictive format would severely limit the potential market. Figure 2 shows input media options for the EMS concept.

An examination of the figure reveals that many of the potential input media – ie, page-like material, microfilm, and punched cards – would involve some type of electro-optical scanning technology to put the message into a format for electronic transmission. It is the page-like material and the scanner technology required to read it that the remainder of this report is concerned with.

EMS GOALS

The phrase "page-like material" can imply many formats such as typed, drawn, or handwritten information of various colors on paper of almost any color and continuous tone pictures that may be in black and white or many colors. The Office of Advanced Mail Systems Development (AMSD) has determined in this initial analysis that it will ultimately be necessary to scan page-like material with these criteria:

1. The data can be in typed, printed, handwritten, or continuous tone form.
2. The text data can be most colors on most colors of paper.
3. The continuous tone data can be black and white or multicolor.
4. The scanning technique must be capable of at least 80 lines per centimetre (200 lines per inch).
5. Within the limits of system resolution, the quality of the reproduced transmitted message must be very nearly equal to that of the original.

In addition to the above input criteria, AMSD has determined that the material must be scanned at a rate equivalent to twenty 8½-by-11-inch pages per second in order to handle the volume anticipated for an EMS system. As a point of comparison messages currently sent by facsimile are handled at a rate of 4800 bits per second. At this bit rate it would take fascimile transmission equipment 78 minutes to transmit a black and white image with EMS quality.

NELC MISSION

The large disparity between existing scanning technology and the goals of the envisioned EMS required the implementation of a major development program. In October 1974 the USPS and NELC signed an agreement in which NELC, primarily the Display Division, agreed to provide technical support for 1 year for the development of scanning technology for the very advanced EMS system. Acceptable progress during 1975 resulted in the issuance of a second agreement for work to begin in October 1975. A

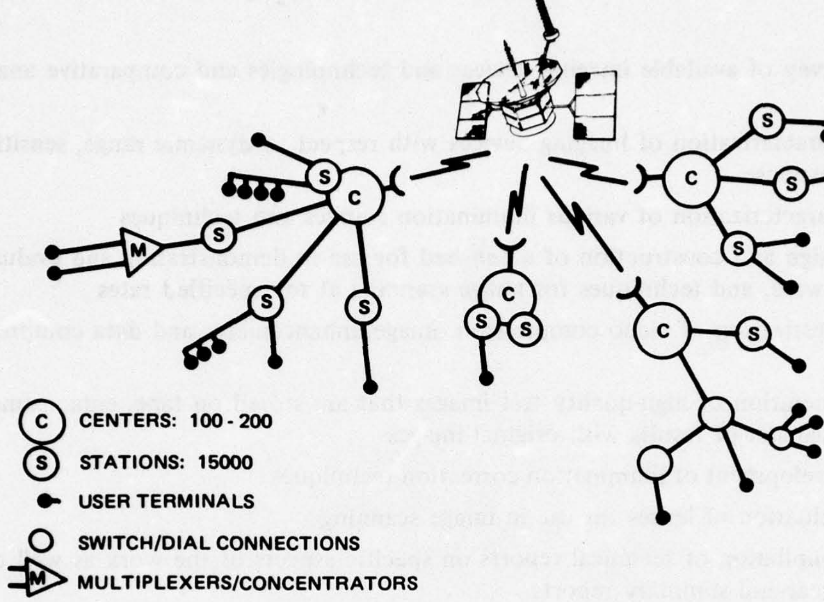

Figure 1. USPS Electronic Message Service.

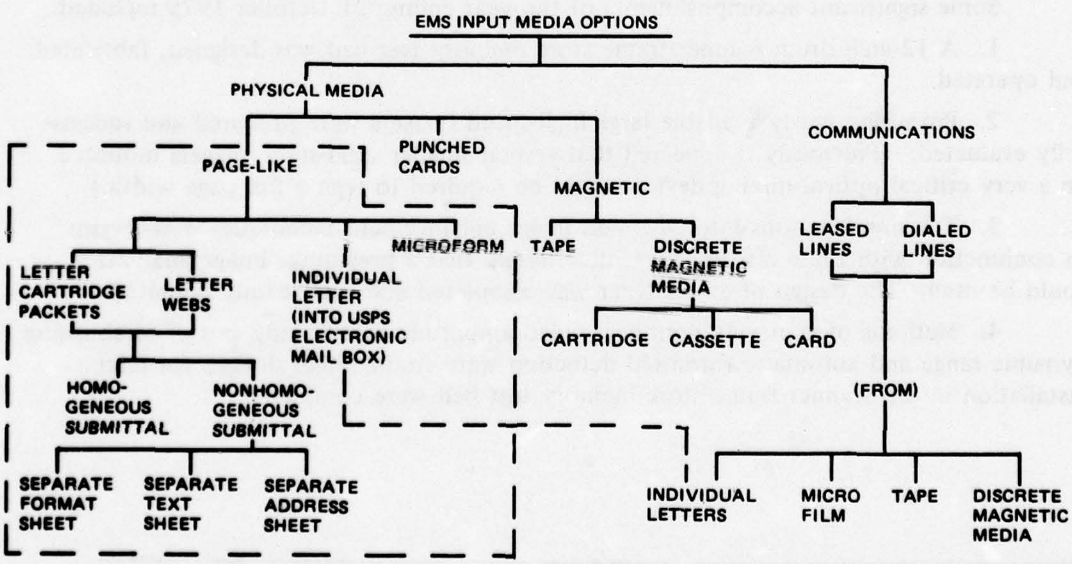

Figure 2. EMS input media options.

report was written to summarize the first year's accomplishments.* This report covers the second year's work beginning 10 October 1975 and ending 9 October 1976.

Tasks performed and services provided by NELC during these 2 years have included:

1. Survey of available imaging devices and technologies and comparative analysis of capabilities

2. Characterization of imaging devices with respect to dynamic range, sensitivity, and spectral response

3. Characterization of various illumination sources and techniques

4. Design and construction of a test bed for use in demonstrating and evaluating hardware, software, and techniques for image scanning at the specified rates

5. Investigation of video compression, image enhancement, and data compression techniques

6. Generation of high-quality test images that are stored on tape; enhancement of data and comparison of results with original images

7. Development of illumination correction techniques

8. Evaluation of lenses for use in image scanning

9. Compilation of technical reports on specific aspects of the work as well as progress and year-end summary reports

10. Consultation and support services including the monitoring of hardware contracts, evaluation of proposals, and writing of procurement specifications

1975 HIGHLIGHTS

Some significant accomplishments of the year ending 21 October 1975 included:

1. A 12-inch drum scanner/frame store memory test bed was designed, fabricated, and operated.

2. Promising newly available large high-speed imagers were procured and successfully evaluated. (Previously it appeared that several smaller solid-state imagers mounted on a very critical optical mixing device would be required to scan a full page width.)

3. The investigations into edge and image enhancement techniques were begun. In conjunction with these efforts it was determined that a prestorage image analyzer could be used. The design of an analyzer was completed and successfully operated.

4. Methods of achieving nonlinear video amplitude partitioning and of establishing dynamic range and automatic threshold detection were studied, and designs for later installation in the scanner/frame store memory test bed were completed.

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*First Annual Report Advanced Mail Systems Scanner Technology, 22 October 1975, prepared by NELC Display Division, NELC TR 1965.

1976 TASKS

For the year ending 9 October 1976, the services performed can be divided into five categories. The categories and the tasks within each are listed below.

Hardware deliverables

- Design and build large drum scanner assembly.
- Improve illumination source.
- Build driver boards for new imagers.
- Design and build peripheral interfaces for test bed.
- Add multimode input to the image analyzer.
- Integrate all hardware units
- Evaluate various imagers and systems.

Software deliverables

- Program high-speed ROMs with microcodes.
- Design and implement system utility programs.
- Design and implement image handling programs.
- Design and implement high-level procedure program.

Document deliverables

- Prestorage processing preliminary report.
- Frame store memory and display memory controller second report.
- Advanced imager summary report.
- Data compression summary report.
- Image enhancement report.
- Reliability/warranty report.

Major procurement contracts

- Imager for time delay integration (TDI) with RCA

Support services

- Provide technical portion of the 4 to 10 pages per second scanner specification for AMSD.
- Review technical section of proposals that were submitted in response to the above scanner specification.
- Provide technical liaison support between various vendors and AMSD.
- Provide technical consultation to AMSD as requested.

Some of the categories of effort involved considerable overlap – notably hardware, software, and documentation. In the next section of this executive summary the first two categories of tasks are described in detail. The material presented for the third category,

document deliverables, will be essentially the results and/or conclusions from each document, because each is included in its entirety as an appendix. The fifth category, support services, is not detailed further.

1977 PLANS

The plans for FY77 will follow much the same format as those for FY76. The categories of work and the tasks within each are listed below.

Hardware deliverables

Obtain and evaluate any new imagers that appear during the year that may be suitable for Postal Service use.

Implement the tracking/TDI mode via test bed hardware and evaluate available devices, including the RCA TC-1155 camera and the new area imager RCA is scheduled to deliver about midyear.

Exploit the frame store memory and its control to achieve elastic buffering, block void encoding, and two-dimensional image enhancement and compression.

Acquire test bed hardware to implement the most promising image enhancement concepts that currently exist in software form.

Investigate the potential for reducing the expected frame store memory capacity requirements by prestorage processing and further exploitation of the image analyzer hardware.

Evaluate techniques for outputting the image data, as stored in the frame store memory, for the purpose of recreating the image on paper (or equivalent).

Software deliverables

Conduct further studies in image enhancement, taking into account FY76 results, and implement findings in software.

Design and implement techniques for investigating in detail various data compression techniques including Walsh, Fourier, slant, and differential pulse code modulation (DPCM).

Document deliverables

Frame store memory and display third report

Advanced imager summary report

Data compression summary report

Advanced prestorage processing report

Monthly progress/technical reports

Third annual report of total program

Major procurement contracts

- **Continue development of the tracking TDI imager.**
- **Investigate possible procurement of laser scanning breadboard hardware for evaluation in EMS systems.**

Support services

- **Provide technical liaison support between various vendors and AMSD.**
- **Provide technical consultation to AMSD as requested.**

TASK SUMMARIES

HARDWARE

LARGE DRUM SCANNER

The year was started using the small drum (12-inch circumference) test bed (SDTB); however, this drum size did not match what Pitney Bowes had selected in their development of paper handling equipment, so design and fabrication of a new compatible large drum test bed (LDTB) were initiated. The LDTB included a 40-inch circumference drum and a Baldwin incremental encoder which put out 8192 pulses per revolution. Drum speeds from 1/5 to 352 revoltuions per minute were provided. The power supplies, imager mount, and card cage were transferred from the SDTB. Fluorescent lamps were installed as the initial illumination light source. The LDTB was put into service in early June and has been used continuously with no further mechanical modifications. Additional details and drawings of the two scanner test beds can be found in appendix C. Figure 3 is a photograph of the hardware being developed for the USPS. The LDTB is located in the right center portion of the photo.

ILLUMINATION

In order to implement the envisioned EMS system, two important considerations exist in the area of illumination: the rate of message handling and the quality of end product. The first item, message rate, implies that more light is required as the page rate increases, and it appears that there are ways of getting more light on the page if it is needed for any particular sensor configuration. However, the second item, a high-quality end product, is of prime concern no matter what the page rate may be. It is the meeting of this goal that has dictated much of the work to be described below. Any variation in light output over the width of a page, if not corrected, ultimately looks like data to the reproducing hardware and thus detracts from the quality of the end product.

The SDTB used a quartz halogen lamp for illumination. For several reasons this type of lamp contributed heavily to poor end product quality. As an alternative source, high-brightness flourescent lamps were evaluated and found to be a significant improvement. These lamps thus became the source used in the LDTB.

The lamps, however, were not the ultimate solution, since there is a consistent dropoff in light gathered by the scanner lens at each end of the scanned line. In order to compensate for this deficiency a software technique was devised to correct for this phenomenon – in fact it corrects for nearly all problems that result in nonuniformity of the sensor portion of the scanning system across the page. The imager scans a high-quality white test target, and the resulting video signal is used to generate a correction factor, pel by pel, for all message data to follow until another correction scan is made. The correction technique makes the system appear to have a perfectly flat response over the width of the page to within ±1/2 least significant bit from the scanner analog-to-digital encoder. Details of the correction technique and the illumination sources are included in appendix C.

LSF 1966-10-76

Figure 3. USPS/NELC test bed.

The illumination problem discussed above applies independently of the color of the image. There is another problem that is color dependent even though the reproduction may be black on white. The fluorescent lamps used were basically green illuminators, and thus if green ink were used in the message being scanned the contrast between the white paper and the green ink would be very low – in the worst case the imager would tell the system a blank page was being scanned. The answer to this problem is to provide either very broadband illumination (white light) or three different colors of illumination (red, green, and blue) and then to select the source that produces the highest contrast. The latter approach is the more desirable one, since an eventual goal of reproducing messages in color is foreseen. In order to pursue this approach, special fluorescent lamps of the high-brightness type were procured from Sylvania containing red, green, and blue phosphors that were mixed in the ratio of 1:2:8, respectively. This ratio compensates for the falloff in sensitivity of the imager from red to blue. The net effect is that the imager produces the same output signal for each color when a white test target is placed on the scanner drum and a red, green, or blue filter is placed in front of the imaging lens. Details on this work are covered in appendix E under the subject of Color Filtering. This area will get much more attention in FY77.

IMAGING DEVICES AND SYSTEMS

Two sizes of CCD imagers were used in the scanner test bed during FY76:

Fairchild CCD-110, a 256x1 pel device

Fairchild CCD-121, a 1728x1 pel device

Problems were encountered with them that have apparently been eliminated in newer versions of these devices and in a completely new device that Fairchild has put on the market, the CCD-131DC. This device has 1024 pels and two output ports that are capable of being clocked at a rate of 12 megapels per second each for an effective rate of 24 megapels per second. Improvements that were made in the Fairchild imager include:

Better arrangements in assigning signals to pins, thus lowering crosstalk levels

Hermetic sealing

Opaque shields over the transfer gates to eliminate peripheral vision

Increasing the saturated output signal voltage to 0.75 volt from 0.200 volt for the CCD-121 and CCD-131

Table 2 in appendix C summarizes the features of the known imagers as of early June 1976 and ranks the devices as to applicability to USPS problems. The emergence of new and improved devices has changed the ranking. Table 1 of this executive summary lists the prime characteristics of the first five devices as of the end of FY76.

Other imager work accomplished during the year involved the evaluation of the RCA TC-1155 television camera that incorporated the SID-51232 surface channel CCD imager. Complete details of this work are contained in appendix C. This imager is of interest because of its possible application to the TDI mode of imager operation which is ranked number 1 in table 1. The SID-51232 tested by NELC had three major deficiencies, two of which were development-oriented and thus probably could be improved to an acceptable level. The third, the need for background bias illumination, was inherent with the type construction and was judged to be highly undesirable.

TABLE 1. RELATIVE APPLICABILITY OF VIDEO SENSORS FOR ELECTRONIC MESSAGE SERVICE.

Device Type, Array Manufacturer, Size	Element Size, mils	Data Rate, ports at megapels per second	Output Amplitude, volt	Abutment Problem	Remarks	Rank
Developmental RCA 750x100	0.6x0.6	4 at 21 each	TBD	none (with 1700-pel version)	Will operate in TDI mode at 20 pages per second	1
CCD-131 DC Fairchild 1024x1	0.51x0.51	2 at 12 each	0.7	minimal, one linear abutment	10 pages per second with two devices Hermetically sealed case	2
RL-1872F 1872x1 Reticon	0.59x0.61	4 at 10 each	–	none	9.5 pages per second max Requires charge amplifier	3
CCD-110F 256x1 Fairchild	0.51x0.63	1 at 10	0.2	difficult, seven linear abutments	19 pages per second with eight devices	4
CCD-121HC 1728x1 Fairchild	0.51x0.67	1 at 1	0.7	none	Good only for slow applications	5

The camera was subsequently returned to RCA for replacement of the imager with an improved type and modification of the camera for use in the TDI mode with the scanner test bed. Since the TDI work had not begun by the end of FY76, no real evaluation of the new imager could be made. It was operated, however, in a superficial way with a strobe light that did verify its functional capability. The TDI mode of operation will be an area of prime importance in FY77 work.

IMAGER DRIVER BOARDS

The SDTB was operated until it was retired with the Fairchild CCD-110 imagers. This scanner assembly served more as a signal source to check out the complete test bed than to evaluate scanners or take data. By the time the LDTB was operational, confidence in the overall system had risen to the point at which operational characteristics of the scanner could be identified and separated from the test bed overall performance. It was determined while using the SDTB that the circuit boards furnished by Fairchild for demonstrating their CCDs were not adequate for the clocking speeds required in the scanner test bed. New CCD driver boards were designed and fabricated using the best in high-speed logic techniques and keeping the analog signals separated from the digital signals. When the Fairchild CCD-121 (1728 pels) was installed and fired up, two peculiarities were noted. They involved changes Fairchild had incorporated into the larger devices. One was solved by adding reverse pulse clamping diodes to the clocking pulses on the circuit board and the other required reverting back to capacitor coupling for the board output amplifier. The improved CCD-121 driver board was subsequently used for about the last half of FY76.

IMAGE ANALYZER MULTIMODE INPUTS

The functional ability of the image analyzer portion of the scanner test bed was expanded early in the year to provide the ability to do "first derivative" statistics (FD stats) and "run length" statistics (RL stats) in addition to the original "pel brightness" statistics (PB stats). The hardware concept changes are detailed in appendix A while the utilization of the hardware is discussed in appendix C. The analyzer performs only one of the three functions at a time on instruction by the frame store memory controller. The operation of each function is performed by hardware processing. As utilized in the USPS/NELC test bed, the analyzer gets its input from raw image data stored on magnetic tape, and the tape must be run through once for each type of statistical data desired.

The image analyzer was developed to accomplish two tasks: to aid the scanner test bed in producing the very best stored image data, and to produce quantitative data about various images for data compression technique development. The first task makes use of the PB stats to expand the dynamic range of the imager video signal so as to just fill the dynamic range of the analog-to-digital converter. The second task requires the use of all three types of statistical data in order to design the method of data compression to be implemented in the hardware.

Several important facts have been obtained from the image analysis/data studies accomplished in FY76. These include

1. Pel brightness statistics for typewritten pages and continuous tone photographs appear to have characteristics sufficiently different that an algorithm could be generated to identify which type of message is being processed.

2. First derivative statistics failed to show expected large differences in adjacent pel brightness levels, which suggests that the imaging lens does not have the resolving power required for 80 pels/cm.

3. Run length statistics showed a very large number of very short runs in the least significant bit planes, which pointed up the unbalanced output from the two analog transport registers of the CCD imager and tended to produce relatively low compression ratios. The new CCD-121H imager should clear up this problem.

4. Variable length coding algorithms exhibited higher compression ratios than fixed length codes.

5. The use of Gray coding produced about 30% more compression with any algorithms than did binary coding.

All the above conclusions are discussed in appendix D in detail; however, it will be FY77 before suggested hardware changes can be made or questions that emerged can be investigated to the point of conclusion.

PERIPHERAL INTERFACES

During FY76 several interface channels were added to the frame store memory controller:

Input and output to a Kennedy model 9000 tape deck via a model 9217 Format Control Unit

Input and output to a Bright model BI-2600 tape deck

Output to a Tektronix model 4632 hard-copy printer

Other channels were expanded in capability:

Input and output to the Tektronix model 4023 computer terminal

Input and output for the imager analyzer FD stats and the RL stats

The output channel for a Conrac RQB-17 monitor was made in FY75 and continues to be used as originally implemented.

The Kennedy tape deck is used as the prime storage element for storing a complete image from the LDTB. It works through the Format Control Unit, which can handle up to four tape decks. Eventually it will be required to drive a second tape deck, because the Bright unit is on temporary loan from other NELC programs. The Bright unit is used for temporary storage in the development of image enhancement techniques and for illumination correction. The Tektronix terminal and printer units are also GFE from other programs. It has been necessary to share these units during the year with the owners, which has caused some minor program workarounds.

SOFTWARE

The USPS/NELC Test Bed is capable of being commanded via the Tektronix 4023 terminal and the Monitor Command Summary instruction set (table 2). This set of instructions is the means by which operational programs are entered and generated. The actual

TABLE 2. MONITOR COMMAND SUMMARY.

TRANSFER (address)	Transfer 64 words from analyzer to location in memory beginning at (address)
TABULATE (address)	Tabulate on terminal display 64 words beginning at (address)
INSPECT AND CHANGE	Allows inspection and change of memory cell from keyboard
GO TO (address)	Transfer program control to (address)
TEXT	Allows entry of textual data for printing on terminal
READ (tape) (address)	Loads data from (tape) to (address)
DATA (address)	Allows entry of a sequence of signed decimal integers at (address)
WRITE (tape) (add) (add)	Write data on (tape) between (address) and (address)
EMC	Enters new monitor command
REWIND (tape)	Rewind specified (tape) to load point
FILEMARK (tape)	Writes filemark on specified (tape)
LIBRARY (tape)	Loads library from specified (tape) into memory and displays page one
SHOW (page)	Displays specified (page) on terminal
UPDATE PAGE (page)	Places terminal display in memory at specified (page) location
UPDATE LIBRARY	Places memory copy of library on tape in library file
HISTOGRAM (dis) (add)	Places 64 histogram values on specified (display) starting from specified memory (address)
POSITION (tape) (file) (rec)	Position specified (tape) to (file) number and (record) number
MOVE (add) (add)	Move data from (address) to (address)
RESET (lib)	Clears all pages of specified (library)
RESET (histogram)	Clears refresh for display
RESET (stats)	Sets (statistical) block in memory to zero
JSR (address)	Selects subroutine at specified (address)
SEARCH (add) (add) (word) (mask)	Modifies all occurrences of a specified bit pattern between (address) and (address)
SBK	Position Kennedy tape at block 1
BBK	Position Kennedy tape at block 1 unless already at beginning of file
SFK	Position Kennedy tape at beginning of next file
BFK	Position Kennedy tape at beginning of current file
STATUS	Displays current position of tape units, contents of various portions of memory, and image display conditions
SET (status)	Set or reset specified (status) line
CONTINUE	Returns program control to any program using the system monitor as a subroutine

operational programs are built up from a set of user accessible instructions referred to as the Macro Instruction Set (table 3). Some of these instructions perform relatively simple tasks, but some are very involved and powerful. For example, instruction 210 captures a complete image from the LDTB and instruction 215 repetitively displays an image on the high-resolution monitor. More detailed descriptions of the macro instructions can be found in appendix B. The complete hierarchy of operational program levels includes:

Microcodes

Macro instructions

Subroutines

Utility programs

Image handling programs

High-level procedure program

All these levels are discussed further in the following sections.

MICROCODES IN HIGH-SPEED ROMs

Each of the macro instructions discussed above essentially calls out the starting address of a set of microcodes stored in PROMs (programmable read only memories). The microcodes contain the actual hardware instruction details necessary to implement the macro instruction. FY76 was started with Intel 1702A UV erasable low-speed PROMs in the memory controller; by midyear these had been replaced with 12 Monolithic Memory 6306-IJ high-speed PROMs that were programmed by the vendor with the microcode data furnished by NELC.

SYSTEM UTILITY PROGRAMS

In developing the program to process the image data in the complete test bed, it was found that there were many small groups of macro instructions that were repeatedly used. These were subsequently organized into a set of "subroutines" that could be called upon much as a microcode. (The final subroutines will be documented in the FY77 Frame Store Memory and Display Report.) Then with the repertoire of macro instructions and subroutines many larger utility programs were developed for manipulating data in memory and on tape including:

Write on tape

Read from tape

Locate specific blocks of data on tape

Move data around on tape

Inspect and change memory word

Search through memory

Program library manipulations

Transfer statistics generated by image analyzer into memory

TABLE 3. MACRO INSTRUCTION SET.

Opcode	Mnemonic	Function	Opcode	Mnemonic	Function
200	LDA	Load A	240	SRO	Shift A right, 1 fill
201	LADAX(X)	Load A indexed	241	SRZ	Shift A right, 0 fill
202	STA	Store A	242	SLZ	Shift A left, 0 fill
203	STAX(X)	Store A indexed	243	SRC	Shift A right, circular
204	LDX(X)	Load index	244	AND	Logical AND
205	STX(X)	Store index	245	IOR	Logical OR
206	LSP	Load stack pointer	246	XOR	Logical XOR
207	LDK(X)	Load K-register	247	COM	Complement
210	CAPT	Capture	250	4DD	Add A
211	CLX(X)	Clear index	251	SUB	Subtract A
212	INX(X)	Increment index	252	INC	Increment A
213	DCX(X)	Decrement index	253	DEC	Decrement A
214	DSZ(X)	DCX, skip 0 result	254	CLA	Clear A
215	DISP	Display	255		
216	HALT	Halt	256	SMC	Set MOS clock
217	NOP	Null operation	257		
220	JP	Jump unconditional	260	MPR(Y)	Memory protect
221	invalid		261	TRAX(X)	Transfer (A) to index
222	invalid		262	TRXA(X)	Transfer (index) to A
223	JNN	Jump A ⩾ 0	263	PUSH	(A) placed on TOS
224	JPN	Jump A < 0	264	POP	(TOS) placed in A
225	JPZ	Jump A = 0	265	LDAC	Load A with constant
226	JNZ	Jump A ≠ 0	266	ADDC	Add constant to A
227	invalid		267	SUBC	Subtract constant from A
230	invalid		270	CAPL	Capture line
231	JPX(X)	Jump indexed	271	OUTV(X)	Output video tape ch x
232	JPA	Jump A	272		
233	BYT	Shift right 8 bits	273	INPT(X)	Input from tape ch x
234	JPI	Jump indirect	274	OUTT(X)	Output to tape ch x
235	JPR	Jump subroutine return	275	INP(X)	Input on ch x
236	JSR	Jump to subroutine	276	OUT(X)	Output on ch x
*237	SKIP	Skip on skip x set	277	SIOC(X)	Skip on I/O cond x

(x) indicates modifier sensitive

* not yet implemented

TOS = top of stack

Display tabular or histogram data on terminal
System status monitoring

IMAGE HANDLING PROGRAMS

Using the macro instruction set, subroutines, and the system utility programs, higher-level programs were developed in FY76 for manipulating, correcting, and analyzing the image data received from the LDTB. It is through the use of these image handling programs that the bulk of the information collected for the USPS is obtained. Programs in the image handling library include:

High-resolution monitor display routines

Image analysis

Image enhancement routines for:

- recursive digital filtering
- nonrecursive enhancement

Logarithmic video compression

Illumination correction

Generation of illumination correction curve

Compression ratio calculations

Reformatting of data to send out for hard-copy processing

Generation of test images for checking various algorithms

The theory, algorithms, and results of the image enhancement programs and logarithmic video compression, along with color filtering and separation, are discussed in detail in the Image Enhancement Report, which is appendix E to this summary report. Major developments reported in appendix E include:

1. The nonrecursive enhancement technique provides symmetry that the recursive filter technique does not.

2. The nonrecursive algorithm appears to give the better enhancement results.

3. The proper choice of color filtering for images other than black and white can greatly enhance the paper-to-ink contrast.

4. A logarithmic compression formula was derived from which commercial logarithmic analog-to-digital converters could be programmed.

5. There is little observed difference between a 6-bit linear and a 5-bit companded image.

6. Four-bit companded images show noticeable contouring.

HIGH-LEVEL PROCEDURE PROGRAM

In order to do a complete image analysis with a minimum of operator attention, various image handling programs were organized into a "high-level procedure program."

This program was used extensively in collecting data for appendix D, the Data Compression Report, and will be used extensively in the future. Because much of the processing involves moving data into and out of magnetic tape storage, a complete run of this program for one image requires about 2-1/2 hours. Major functions of this program include:

Set up the Kennedy tape for accepting data from memory.

Capture white standard from LDTB and store on tape.

Capture image from LDTB and store on tape.

Using white standard data, correct image data for illumination nonuniformity.

Transfer image data between tape units as required for image processing.

Instruct image analyzer for all statistical data gathering functions.

Store, display, and/or print statistical data generated by imager analyzer.

DOCUMENTATION

During the year monthly progress/technical reports and six specific subject technical reports were written and submitted to AMSD. The reports and dates of publication are:

A.	Prestorage Processing Preliminary Report	26 May 1976
B.	Frame Store Memory and Display Second Report	22 May 1976
C.	Advanced Imager Summary Report	28 June 1976
D.	Data Compression Summary Report	October 1976
E.	Image Enhancement Report	October 1976
F.	Reliability Prediction Report on the Scanning Imager Electronics	September 1976

These reports are included in their entirety as appendixes A through F to this annual report. The subject matter, results, and conclusions of the first five appendixes have been discussed in earlier sections of this executive summary. The Reliability Prediction Report, appendix F, discussed the reliability aspects of a hypothetical scanning imager electronics system such as might be used in an EMS system. The hypothetical system was patterned after the equipment developed here at NELC but expanded to handle an entire page. Conclusions reached in this report included:

1. The MTBF (mean time between failures) of the hypothetical system was 82 hours with the 4000-bit MOS memory chips NELC is presently using.

2. The principal contributor to the low MTBF is the large number of memory chips – 6000 in the hypothetical system.

3. The MTBF could be raised to 246 hours by using 64000-bit MOS memory chips, thus reducing the 6000 chips in the memory to 375.

4. The MTBF could be increased to over 1200 hours by switching to an integrated injection logic (I^2L) memory device.

5. The reliability of the imaging device does not measurably alter the MTBF of the model equipment.

The above conclusions are theoretical calculations; however, they are based on models presented in MIL-Handbook-217, the standard accepted by DoD as the guide for all military electronics equipment reliability predictions. Note that the very nature of this handbook requires that it be conservative. About nine failures in 1475 hours of operation were predicted by the use of its models for the equipment here at NELC. Only one was actually experienced within that period of operation.

CONTRACTS

The only contract issued by NELC during FY76 for USPS work was with RCA Princeton for development of a tracking/TDI imager. The imager will be 96 pels high by 748 pels wide and will have four output ports capable of being clocked at 21 megapels per second each. As of this report the fabrication technology and porting techniques to be used have been determined. RCA is currently in the process of making the numerous photo masks required to build the imager. The contract will be culminated in the first half of FY77 with the delivery of operating devices.

APPENDIX A: PRESTORAGE PROCESSING

Prepared

for

US POSTAL SERVICE

May 1976

by
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NAVAL ELECTRONICS LABORATORY CENTER
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ACKNOWLEDGMENT

The author gratefully acknowledges the contributions on prescanner image analysis from AD Gomez.

INTRODUCTION

Prestorage processing is an important adjunct to image acquisition for a number of reasons. By definition, prestorage processing includes any intentional augmentation of image data prior to acceptance of the data into the frame storage buffer memory. This processing includes prescanner strategies to determine optimum color of illumination for the main scanner, accumulation of statistical data pertaining to the distribution of reflection densities of the copy, image enhancement algorithms which can be executed in real time "on the fly" without requiring buffer storage, and any of a number of compression techniques which can reduce the final required capacity of the frame storage memory.

This report is devoted to a description of the design and application of an image analyzer. The subjects of image enhancement and data compression, which may also be accomplished by prestorage processing, are covered separately in subsequent detailed technical summary reports.

It should be emphasized that the image analyzer described herein is a highly complex and versatile subsystem of the USPS/NELC image acquisition test bed. Its purpose is to identify and exploit those parameters of various image types which may be used to optimize the acquisition, storage, and compressibility of the image data.

If and when successful algorithms are developed which meet these goals, it is planned that specifications for simple hardware/software equipment can be generated. Until such time the image analyzer offers a unique high-speed image analysis capability not found in literature describing the capabilities of any other image processing facility.

RELEVANCE TO MILITARY APPLICATIONS

The word image is used in the name "image analyzer" because that is the dedicated function for which the equipment was designed. It can also be used for the tabulation of the frequency of occurrence of up to 2^{24} events in any equipment or system at frequencies up to about 21 megahertz. Time interval statistics can be acquired by using the run length counter mode. The first derivative mode can be a valuable asset in analizing data for the design of nonlinear delta modulation systems.

IMAGE ACQUISITION SYSTEM

A diagram of an advanced electronic message input terminal is shown in figure A1. Only those portions pertaining to prestorage processing will be described here. As shown in the diagram, 8 1/2-by-11-inch copy is input to the system at a rate of 240 inches per second or a page rate of 20 pages per second. At the prescan station there are three image sensors – one with red illumination, another with green, and a third with blue. The three colors of illumination will be used for possible contrast improvement and for future color applications.

Each of the three outputs from these sensors is fed into a preamplifier with fixed gain and offset. The gain and offset on all three preamplifiers are adjusted so that when black velvet, with the lowest possible reflectance, is placed in front of the image sensors, the resulting output from the preamplifiers will produce an

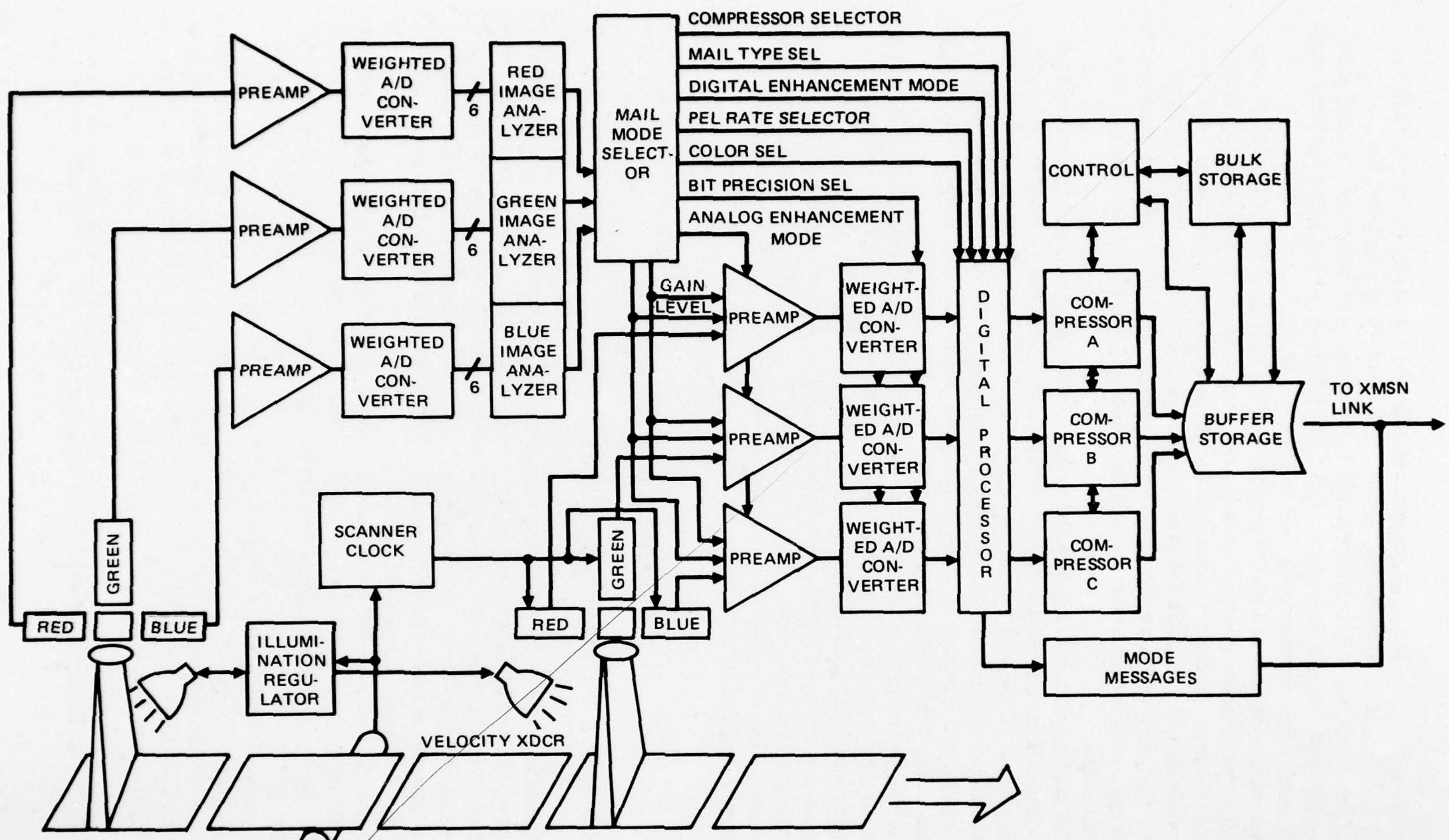


Figure A1. Advanced electronic message input terminal.

output of all zeros from the A/D converters; and when a white surface of $BaSO_4$ with the highest possible reflectance, is placed in front of the sensors, the resulting outputs from the A/D converters will be all ones. The weighted, or nonlinear, A/D converters will convert data according to Weber's* rule to minimize the total number of bits needed to represent each picture element, or pel.

The image analyzer is a statistics gathering machine used to supply image data to the mail mode selector where various decisions are made to properly set up system controls for the main scanner stations. At the present time a requirement is seen to generate statistics which include pel brightness statistics (PBS), run length statistics (RLS), and first derivative statistics (FDS). Preliminary tests may generate requirements for additional statistics which may include time-dependent statistics and various two-dimensional codes.

The mail mode selector is a decision unit for the main scanner system control. It accepts inputs from the image analyzer and uses them for the following: gain and offset adjustments of the main scanner preamplifiers; selection of enhancement modes, which may be either digital or analog; selection of type of data compression; selection of bit precision; and selection of image resolution. These decisions will be discussed in more detail in the following section.

The image analyzer in the advanced electronic message input terminal as proposed must analyze data from the three image sensors at the prescan station simultaneously. It must accumulate all types of statistics simultaneously. The NELC image analyzer to be discussed is designed for one input channel and to accumulate the different types of statistics, one at a time. It is designed to accept data at a channel rate of 21 megapels per second. Four or more channels will be required to produce the total 84 megapel per second design goal.

PRESCANNER IMAGE ANALYSIS

EXPECTED BLACK ON WHITE HISTOGRAM

Models are used in the following discussion for handwritten or typed pages which are composed of ideal black ink on a white background. This model assumes only very small variations in the uniformity of the background and the ink within a line or character. This ideal image model will be defined as one which contains no white noise due to the scanner or any imperfections in the character edge other than minor variations of black intensity due to print ink.

Figure A2 indicates the construction of an ideal histogram defining the areas of the typewritten model which are responsible for the various regions of the histogram. Curve A in figure A2 can be explained in terms of a random relationship existing between a pel and the edge of the character. It is reasonable to assume that there is an equal likelihood of a pel being overlapped with respect to the printed character edge which will create all levels of gray that would exist between the blackest average level of the print and the whitest average level encountered in a page. The expected curve A will be somewhat independent of pel size but will be related to the number of edges found in a particular image.

---

*Not Weber's fraction, but a geometrically proportional step increase for successive Gray levels.

Curve B is the result of the percentage of the page covered by typewritten information. The horizontal width of the distribution B will be proportional to the variations in the black level found in any character and somewhat associated with those pel levels which are related to the registration ratio of black and white at a character edge. The amplitude of the B curve will be dependent upon the resolution at which the image is taken. In the ideal case in which extremely high resolution is utilized, the amplitude of the B curve would be its greatest and the width would be its smallest. As pel resolution is decreased, the peak amplitude achieved is expected to degrade and the width of the B curve to increase.

The C curve shown in figure A2 is related to the background of the typewritten information. Since this is related to the texture of the paper and illumination uniformity, the width of the curve will be proportional to the variation of reflectivity associated with both small and large displacements on the paper. The small displacement variations are basically due to the grain and texture of the paper, watermarks, and other identifying properties incorporated in the paper structure. The peak value of C will be directly related to the width of the curve. Since the total number of white pels due to the background will be a known number, the resulting total area under the C curve will remain equal to this number. Since the percent of a typewritten page which is black is generally small, the ratio of the areas of the B and C curves will be directly related to the print density on the page. As a first-order approximation, the ratio of the area of curve B to C will be in the ratio of the area of the page covered by characters to the whole page. With these ideal estimates of the properties that are expected to be found in a typewritten image, it is possible to search the data for these properties and determine the validity of this model.

EXPECTED CONTINUOUS TONE HISTOGRAM

Figure A3 shows an ideal continuous tone pel brightness histogram taken for the pel levels expected to be encountered for a nominal ideal image model. The predominant factor which distinguishes the continuous tone image from the typewritten image is the difference in white level that would be expected on the continuous tone image. Since a typewritten page is composed principally of a background which is one shade of white, a photograph is expected to contain more intermediate dark areas. Figure A3 depicts a higher number of black tones in the image than white. If the image contains sharp edges or boundaries, again as in figure A2, an A curve will be generated which will be related to the number of boundary edges that are found on the image. The remaining events when added to the A curve generate the D curve, which represents the total normalized number of occurrences at each pel level for the envisioned model.

EXPLOITATION OF HISTOGRAM DIFFERENCES

To create all the control lines necessary to operate the image processing system, the mail mode selector shown in figure A1 is flow diagrammed in figure A4. Starting with inputs from the red, green, and blue image analyzers, the mail mode selector is the source of the required output control signals which configure the main scanner electronics.

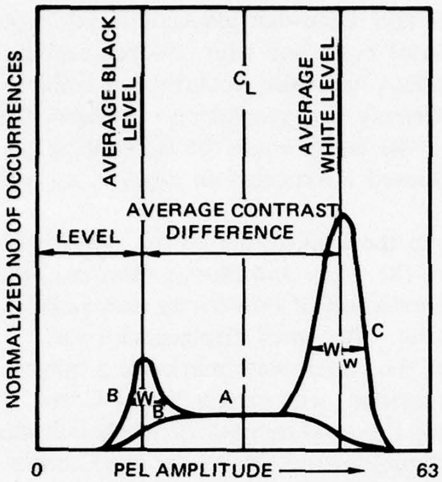


Figure A2. Ideal typewritten image pel brightness histogram.

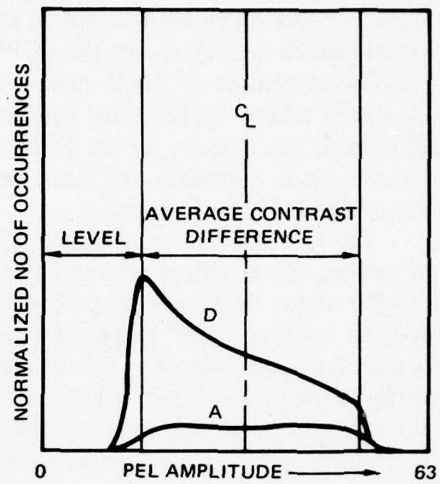


Figure A3. Ideal continuous tone pel brightness histogram.

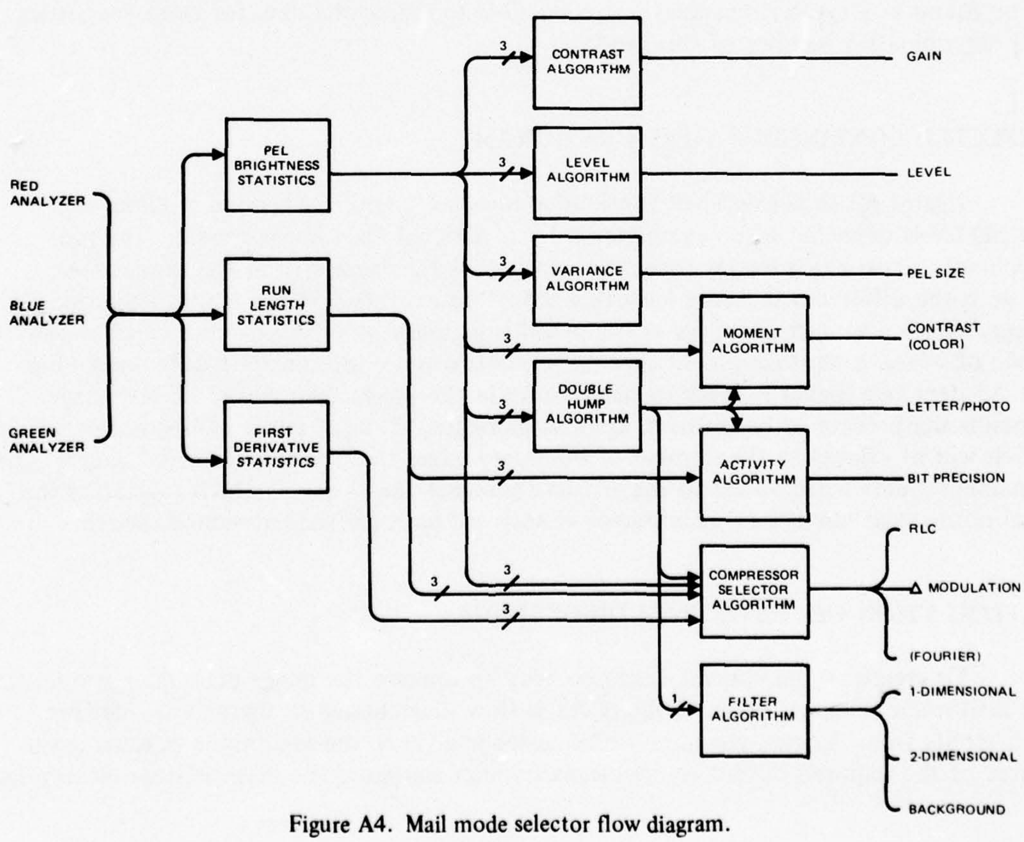


Figure A4. Mail mode selector flow diagram.

The flow diagram of figure A4 indicates the source inputs of the red, blue, and green analyzers which are hardware mechanizations that create pel brightness statistics, run length statistics, and first derivative statistics on the prescanned image. These are shown as being performed in three colors for each operation. The conclusions obtained from this investigation will provide a decision as to whether or not data in this volume are needed. The results from the R, G, and B statistics will be used by the following hardware algorithms, which in turn will generate the required control functions. These control functions will organize the main scanner electronics to accommodate the image in the best possible manner. The following will treat the individual approaches that will be taken in the creation of the various algorithms for the specific controls required.

GAIN

To control the gain for the analog amplifiers that follow the main scanner electronics, a contrast algorithm is to be used. Referring to figure A2 of the ideal typewritten image, the contrast difference is defined as the signal level between the average black print level and the average white background level of the image. The statistics derived from the prescanner will allow the determination of the range of the average black to average white level, and from this the gain will be set for the analog amplifiers in the main scanners. The gain adjustment will have a resolution equal to the prescanner A/D converter resolution.

LEVEL

The level algorithms will be developed in the same manner as the contrast algorithms. Examining figure A2 shows the average black print level is offset from zero by a magnitude which is equal to the level. This level adjustment will allow the range of the A/D converter to be offset so that the full dynamic range of the converter can be matched to the image. The main scanner analog amplifier electronics will be set by the output from this algorithm in increments of n, where n is a binary resolution determined by the prescanner A/D converter.

PEL SIZE

The pel size for the main scanner has been selected to achieve the appropriate resolution of 200 pels per inch for typewritten information. When information with a lower resolution requirement is inserted into the system, it would be of value to reduce the number of pels taken in order to reduce the number of bits required for transmission. To achieve this, a number of approaches will be investigated. One method would be the removal of alternate pels along the line for each line thus reducing the number of pels taken by a factor of 2. The second approach would be to delete adjacent pels on a line and the following line thereby reducing by a factor of 4 the number of pels taken. To make the necessary machine determinations to allow reduction in the number of pels taken, the pel brightness statistics would be examined for their area distribution. The type of relationship to be used for determination of pel size would be based on

the variances determined by examination of the image histogram taken at different resolutions. As an example, consider figure A2 with the ideal typewritten image. If the number of pels taken per page exceeded the resolution required by the image content, the A curve would remain virtually unchanged. For resolutions at which the width of the B curve would decrease, the decrease would occur as a result of a higher number of occurrences of pels with a full black value. Once the information has been normalized, the net effect would be reduction in the width of the B curve. Detailed examination of the variances of the pel brightness statistics taken with different pel resolutions would result in a measure of the differences in the shape of the histograms. This in turn could be used as a method of adjusting the pel size.

CONTRAST

With images being taken in three colors by the prescanner, the image with the best contrast should be selected for transmission. To determine whether the image from the red channel is of higher contrast than the image from the green, an algorithm must be created which will examine the histogram structure and look for information which will identify this distinction. One possible method involves computing the moment of the histogram with respect to the center of the contrast difference. Two important parameters are expected to vary when the color illumination is changed. First is the position in the pel brightness histogram of the substrate reflectance; and second is the histogram location of the average typewritten print reflectance. Two facts are expected when the same image taken in three different colors is examined. The expected result is the creation of three different average contrast differences, and the resulting three relative shapes of both the B and the C curves of figure A2 will in fact be different. If a centerline is erected midway along the average contrast difference and the histogram to the left and to the right for all three colors is adjusted by normalizing until the same average contrast difference occurs at each color, then only the moment of the data with respect to the centerline will be significant in determining which of the images is the most distinctive in contrast. Examples of this type of calculation must be programmed on the frame store memory controller to generate the conclusions for this speculation.

LETTER/PHOTOGRAPH CONTROL

One of the important distinctions to be made by the equipment before processing information is whether it is dealing with a photograph or with a letter. Figures A2 and A3 indicate the expected behavior of pel brightness histograms given typewritten and continuous tone images. The distinctive characteristic of two peaks occurring in the histogram of typewritten information may be found in continuous tone imagery. However, a very distinctive property of typewritten data is the preponderance of white which should occur within the image. In a continuous tone image, in general, we expect to find far fewer white pels in the total image. By comparing the properties indicated in figures A2 and A3, this distinction can be observed. The algorithm to be generated therefore must examine the number of pels to the left of the average contrast difference centerline and compare against the number of pels which are to the right of the centerline. After testing a variety of images, suitable criteria for adjustment of this threshold for determination should be possible.

BIT PRECISION

One of the important parameters to be considered in reducing the number of bits required to transmit an image is the number of bits used to symbolize each pel in the image. The simplest possible scheme that will be evaluated will examine the activity of the run length statistics in each bit plane. The expectation is that the lesser significant bits of a given image will show a high occurrence rate for very short runs, whereas in the more significant bits there should be a high occurrence of long runs. By examining this activity in the run length statistics for each bit plane, a threshold will be sought which will allow an automatic determination at what bit precision a particular image should be executed. Since letter information will ultimately be processed in binary configuration, the bit precision control is intended to be activated for continuous tone information. A completely different technique will be used for the binary decision processing of letter mail.

COMPRESSION

From the brightness statistics, the run length statistics, and the first derivative statistics it is possible to calculate the entropy associated with each process. From a technology standpoint this information will be utilized in determining the magnitude of, and therefore the boundaries for, the compression of data from each of the three techniques. In addition to this information, the first derivative statistics, the run length statistics, and the brightness statistics will be compared to determine which type of coding scheme is optimum for mail transmission. Three techniques of coding which will be evaluated in this manner include run length coding, delta modulation, and a block coding technique. As an example of block coding, a Fourier analysis technique looks very promising.

FILTERING

The filter algorithm would be applied to the image when it is a letter and would be used to enhance the character edges. The techniques to be examined for filtering in two dimensions were reported in detail in the first annual report.

NELC DIGITAL IMAGE ANALYZER

GENERAL DESCRIPTION

The NELC Digital Image Analyzer (DIA) is a 3 1/2-by-19-inch rack mount unit which is constructed via 10000 series emitter coupled logic (ECL) on Augat multilayered wire wrap logic planes. Photographs of the analyzer are shown in figures A5 and A6. The analyzer is designed to generate several types of image statistics in a sequential manner, which include pel brightness statistics (PBS), run length statistics (RLS), and first derivative statistics (FDS). There are two interfaces to the analyzer; one is the high-speed image data input port with all inputs ECL compatible. At present this interface will

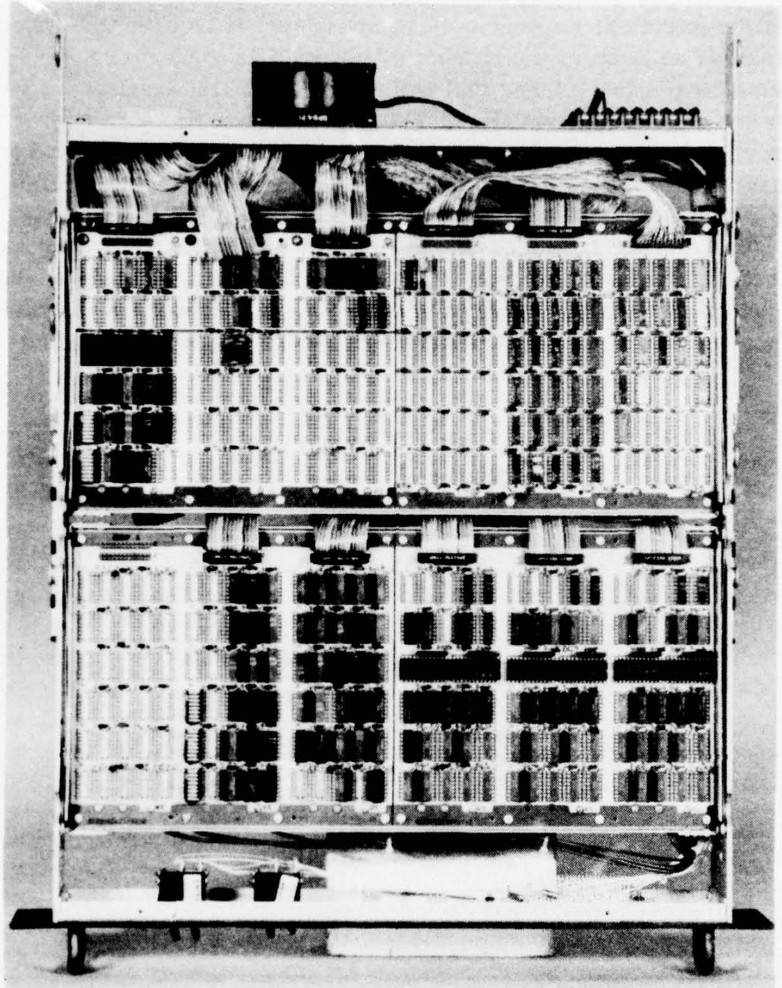


Figure A-5. Digital image analyzer, top view.

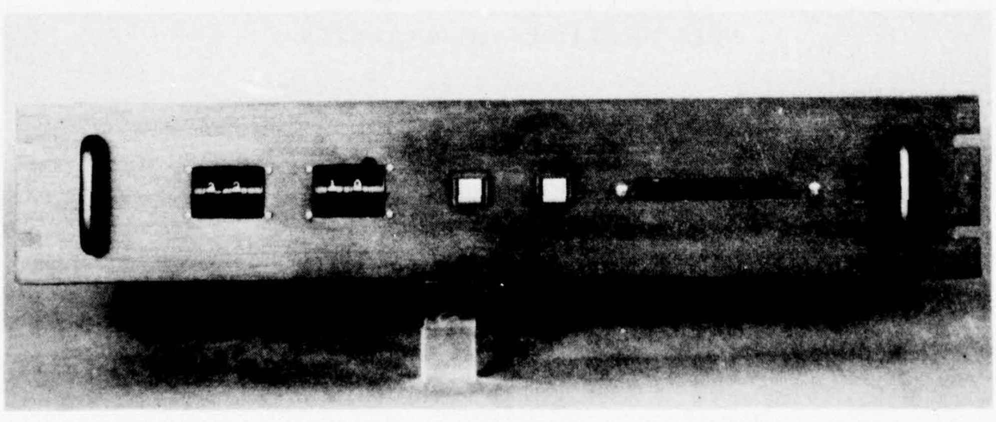


Figure A6. Digital image analyzer, front view.

accommodate image data from the USPS Large Drum Test Bed (LDTB) and the NELC Video Transmission System. The second interface is a general-purpose digital controller interface whose inputs and outputs are TTL compatible. This interface allows operation of the DIA as a peripheral device. It is presently interfaced to the USPS Frame Store Memory Controller (FSMC). A simplified block diagram is shown in figure A7. The image data input to the analyzer is converted to Gray code, which allows operation on either binary or Gray code image data. The mode selector selects from top to bottom pel intensity statistics, run length statistics, or first derivative statistics. The selected output is used as a 6-bit address to a high-speed ECL random access memory organized as 64 words by 24 bits per word. Using this address, the contents of the selected memory location are output, incremented by one, and returned to the same memory location.

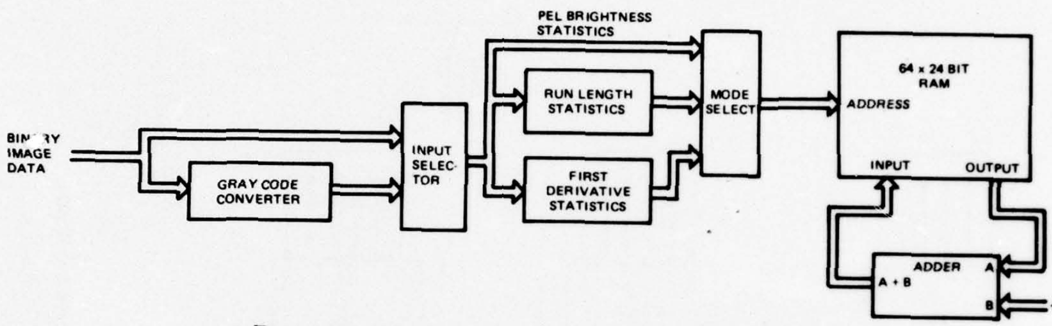
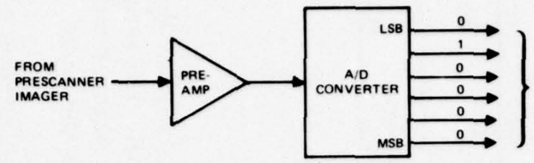


Figure A7. Digital image analyzer simplified block diagram.

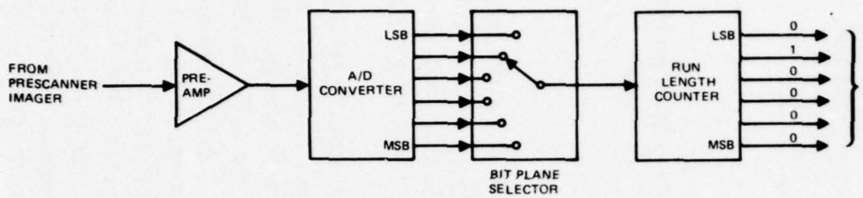
MODES OF OPERATION

The image analyzer will generate statistics on any 6-bit input data format. However, units currently interfaced with the analyzer use a 6-bit binary format. The analyzer is capable of converting binary information to Gray code in order to investigate possible improvement in data compression. All subsequent modes discussed allow the use of either binary or Gray code data for analysis.

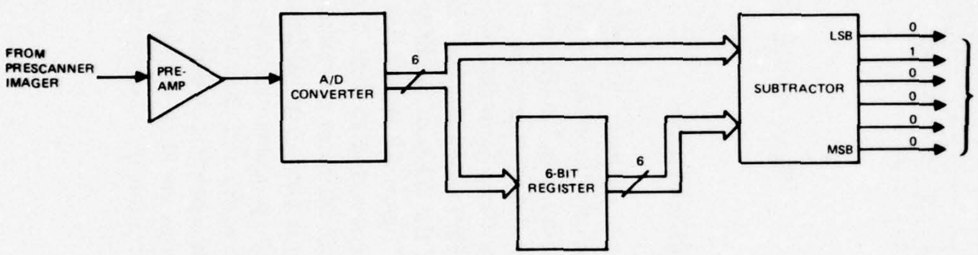
In the PBS mode the analyzer accumulates the total number of occurrences of pels at each of the 64 possible brightness levels throughout an entire image. The upper left portion of figure A8 shows this operation pictorially. Image data from the sensor are amplified and converted to digital format in the A/D converter. The output is a 6-bit binary code with all zeros representing a black pel and all ones representing a white pel. This 6-bit code is used as an address to select one of 64 memory locations in the high-speed ECL random access memory. The contents are read out and incremented by one in a high-speed adder and then stored back in the same memory location. This operation is done on a pel-by-pel basis throughout the entire image. The contents of the 64 memory locations are then read out either manually from an LED display or by the FSMC for generation of a histogram or bar graph display of the information.



Pel Brightness Statistics



Run Length Statistics



First Derivative Statistics

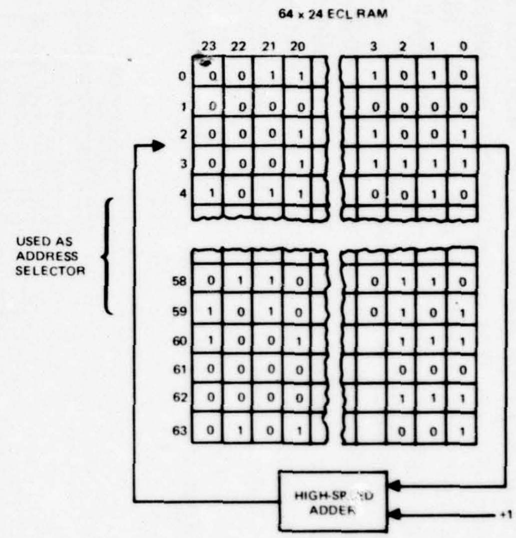


Figure A8. DIA Operating Modes

HARDWARE DESCRIPTION

Figure A9 is a block diagram of the Digital Image Analyzer (DIA). There are two data sources input to the data source multiplexer, one from the high-speed scanner input port and one from the digital controller interface. The selected binary data are then fed into the input selector multiplexer and the binary-to-Gray code converter. The input selector selects either binary or Gray code image data for analysis. The mode selector selects one of the three types of statistics to be accumulated by the analyzer, which are the FDS, RLS, and PBS. The output from the mode selector is strobed into a 6-bit pipeline register for data resynchronization. From this register alternate pels are strobed into each of the two 6-bit data registers organized as a Ping-Pong register whose outputs are alternately selected by the address selector for reading and writing data into the random access memory (RAM). After statistics have been gathered, the address selector selects the interrogate address input for reading data out of the RAM. There are two sources for the interrogation address, one from a manual entry from the front panel and the other from the digital controller interface. The last input to the address selector is from a control counter which is used for clearing the memory and also for diagnostic purposes. The 64-word by 24-bit RAM is used for accumulation of statistics. The data multiplexer selects data from one of three sources for input to the read data register. They are the RAM output data, the write data register output, and an external 24-bit input bus, which currently is controlled manually by a series of switches. Data stored in the read data register are input to the arithmetic logic unit (ALU), the LED display, and the digital controller interface. The ALU is capable of performing 32 arithmetic and logic functions on two 24-bit data words. The write data register stores the output information from the ALU for writing into memory. The LED display provides manual readout of the contents of the RAM. The digital controller interface allows the FSMC to read the contents of the RAM and display them in histogram form on a CRT display. The interface also allows the memory controller to transfer image data from either the 3-megabit frame store memory or magnetic tape to the analyzer for analysis.

FRONT PANEL CONTROLS

Figure A10 is a diagram of the various front panel controls on the DIA. On the left is a 2-digit octal lever switch used for selection of any one of up to 64 operating modes. See table A1 for the modes implemented. The next 2-digit octal lever switch selects any one of the 64 memory locations for manual readout of memory and for various diagnostic modes. The execute pushbutton is used to initiate the various diagnostic modes. The master reset pushbutton is used to clear various portions of the circuitry. On the right is an 8-digit octal LED display used to read data from the memory. There is an additional mode which is designed to check the repeatability or the stability of an image sensor. Assuming that the pel brightness statistics were just accumulated, this new subtract mode may be run in which the memory location is decremented by one instead of incremented as in the previous mode. If the two images were identical, all memory locations should be decremented to exactly zero. In this way the differences in an image, from one scan to the next, will be shown by the resulting information left in the memory.

In the run length statistics (RLS) mode, the analyzer accumulates totals of either zero runs or one runs in an image. The middle left portion of figure A8 describes this

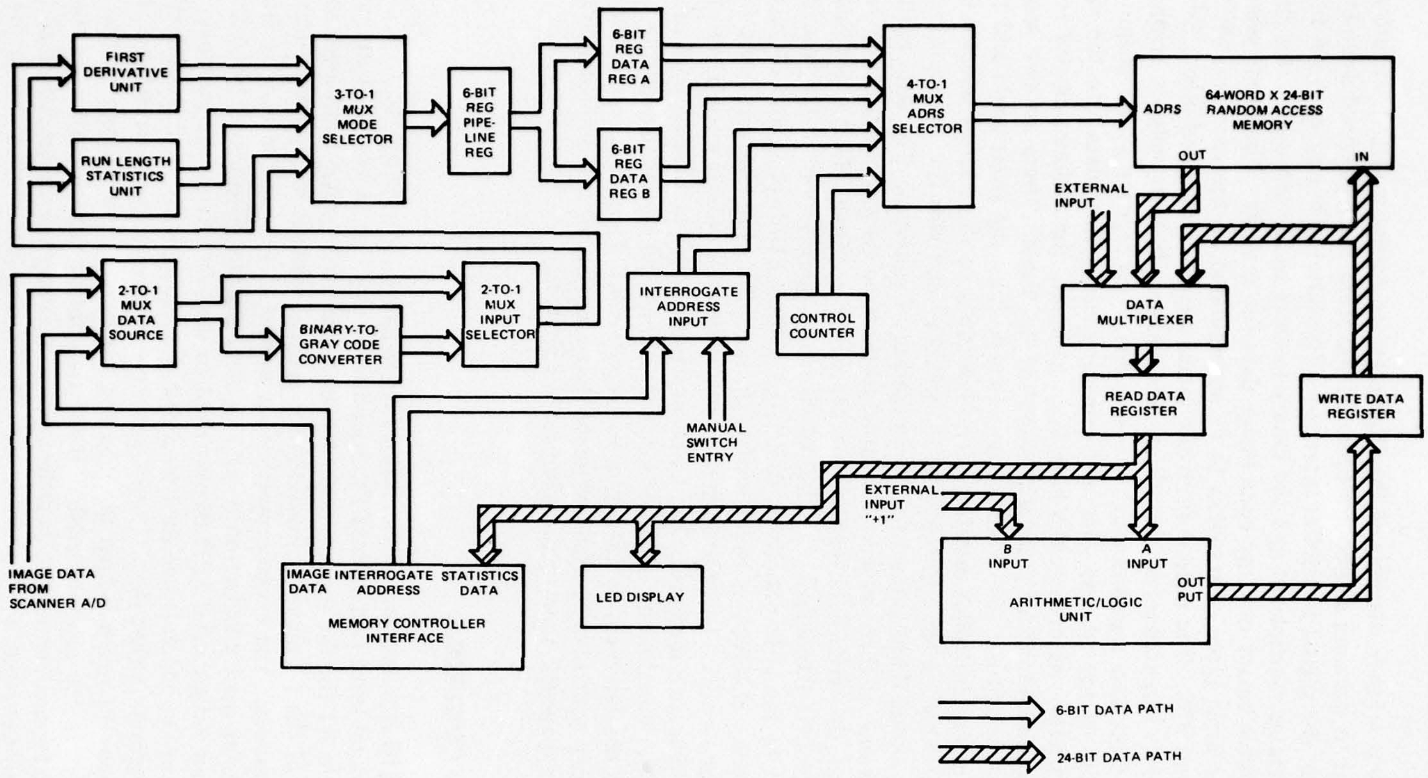


Figure A9. DIA, block diagram.

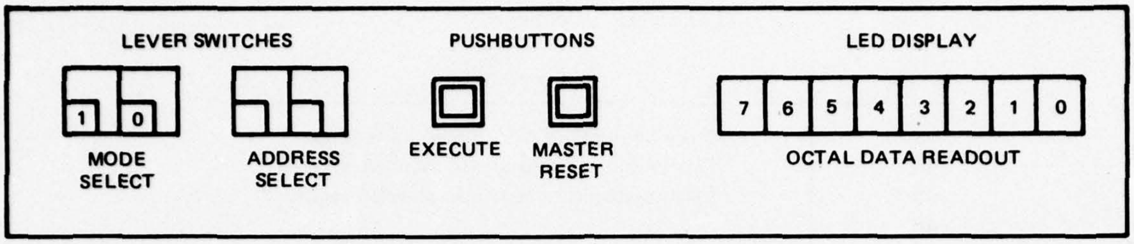


Figure A10. Front panel controls.

TABLE A1. IMAGE ANALYZER MODES.

Mode	Description
00	PBS Binary
01	RLS Binary 0-Runs BP-1 (LSB)
02	RLS Binary 0-Runs BP-2
03	RLS Binary 0-Runs BP-3
04	RLS Binary 0-Runs BP-4
05	RLS Binary 0-Runs BP-5
06	RLS Binary 0-Runs BP-6 (MSB)
07	FDS Binary
10	PBS Binary Subtract mode
11	RLS Binary 1-Runs BP-1
12	RLS Binary 1-Runs BP-2
13	RLS Binary 1-Runs BP-3
14	RLS Binary 1-Runs BP-4
15	RLS Binary 1-Runs BP-5
16	RLS Binary 1-Runs BP-6
17	Not used
20	PBS Gray
21	RLS Gray 0-Runs BP-1
22	RLS Gray 0-Runs BP-2
23	RLS Gray 0-Runs BP-3
24	RLS Gray 0-Runs BP-4
25	RLS Gray 0-Runs BP-5
26	RLS Gray 0-Runs BP-6
27	FDS Gray
30	PBS Gray Subtract mode
31	RLS Gray 1-Runs BP-1
32	RLS Gray 1-Runs BP-2
33	RLS Gray 1-Runs BP-3
34	RLS Gray 1-Runs BP-4
35	RLS Gray 1-Runs BP-5
36	RLS Gray 1-Runs BP-6
37	Not used
40	Display contents of selected register
41	Clear Memory
42	Store contents of "A" bus in selected register

TABLE A1. (Continued)

Mode	Description
43	Store contents of "A" bus in all registers
44	Continuous increment into selected register
45	Continuous decrement into selected register
46	
.	Not used
.	
76	
77	Analyzer under digital interface control

Notes: PBS Pel Brightness Statistics
RLS Run Length Statistics
FDS First Derivative Statistics

operation. Data output from the A/D converter are fed through a bit plane selector since only one bit stream at a time may be operated on. The output from the bit plane selector is fed into a counter which counts runs of either zeros or ones depending on the particular mode selected. At the end of a run, the count contained in the 6-bit counter is used as an address to select one of the 64 memory locations as in the PBS mode. There is the limitation, however, of only a 6-bit counter, which means that runs of length greater than 64 will have the result that multiple runs are counted. This is true, however, with any run length encoding data compression scheme. For example, if there was a run of 66, memory location 63 and memory location 1 would each be incremented. Note that run lengths of 1 through 64 correspond to memory locations numbered 0 through 63. In the image analyzer there are 24 individual modes to accumulate run length statistics. There are six bit planes and modes to accumulate statistics on zero runs and on one runs. Each of these may be accumulated using the binary code input or Gray code input, resulting in a total of 24 modes.

The first derivative statistics (FDS) modes compute the absolute value of the differences between successive pels in an image. The lower portion of figure A8 shows the operation of the FDS modes. Image data from the A/D converter are input to both a 6-bit storage register and a subtractor. The storage register contains the previous pel value, which is subtracted from the present value to obtain the difference. This difference is used then as an address to the 64-location random access memory as in the previous modes.

There are several other modes of operation for the image analyzer. One of these is the display memory mode. In this mode front panel switch inputs are used to address each of the 64 memory locations to read out the contents on an 8-digit octal light-emitting diode (LED) display. This information can also be read out through a general-purpose digital controller interface under program control. Other modes are designed primarily for diagnostics; they include loading one or all memory locations from a manually switched input bus, a clear memory mode, and continuous count modes to check the arithmetic logic unit and register operation.

HIGH-SPEED DATA INPUT PORT

This interface is comprised of 10 ECL compatible differential signals transmitted over twisted-pair lines. There are six data inputs, a clock, an enable, and a clear memory signal with an echo output response after the memory is cleared. The maximum clock rate to the analyzer is approximately 21 MHz. Currently the analyzer is interfaced via this data input port to the USPS LDTB and to the VTS.

DATA INPUT SELECTION AND CONVERSION UNIT

A block diagram of this circuitry is shown in figure A11. The data source multiplexer selects image data from either the high-speed scanner interface or the digital controller interface. The selected data are then fed into an input selector multiplexer and to the binary-to-Gray code converter. The input selector, which is controlled by the mode switch, selects either binary or Gray code image data for analysis.

FIRST DERIVATIVE STATISTICS UNIT

The first derivative statistics unit computes the absolute value of the difference between successive pel brightness levels. The block diagram of the circuitry is shown in figure A12. There are two 6-bit data registers which contain at any given time the two most recent pel brightness values. Outputs from these registers are fed into both a comparator and a subtractor unit. The comparator decides which value is larger, and the output from the comparator tells the subtractor to subtract A-B or B-A to obtain the absolute value. The output from the subtractor then is used as a 6-bit address to the RAM for statistics accumulation. The basic timing diagram shown in figure A13 illustrates the operation of these circuits. At time interval A , registers A and B contain pel intensity values of 16 and 3, respectively. The output from the comparator is such that A is greater than B, and this control is used to set up an A-B subtract mode. The next clock pulse will load the output from the subtractor into the pipeline register shown in the block diagram in figure A9. At time interval B , registers A and B contain values 10 and 32, respectively. In this case the comparator output indicates that B is greater than A and tells the subtractor to subtract A from B; thus, on the next clock pulse the value 22 is loaded into the pipeline register. In this way statistics are accumulated on the number of occurrences of pel-to-pel differences of magnitude 0 to 63.

RUN LENGTH STATISTICS UNIT

The run length statistics modes are designed to accumulate the number of occurrences of runs varying in length from 1 to 64 as they occur on a particular bit plane throughout an image. Only runs of ones or runs of zeros may be accumulated for a particular image. A block diagram of the run length statistics unit is shown in figure A14. Inputs to this unit include the 6-bit binary or Gray code image data, 3-bit plane control lines which select one of the six bit planes, and a control line selecting accumulation of zero or one runs throughout the image. The selected bit plane output is fed into a data

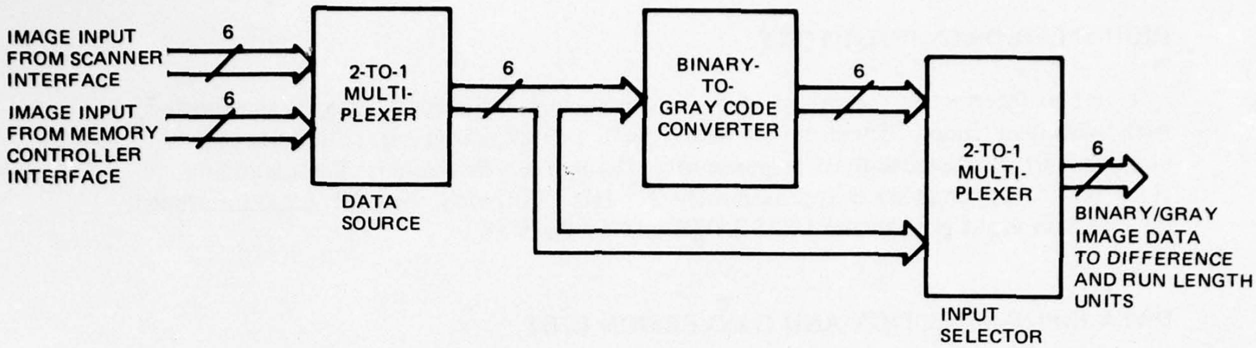


Figure A11. Data input selection and conversion unit.

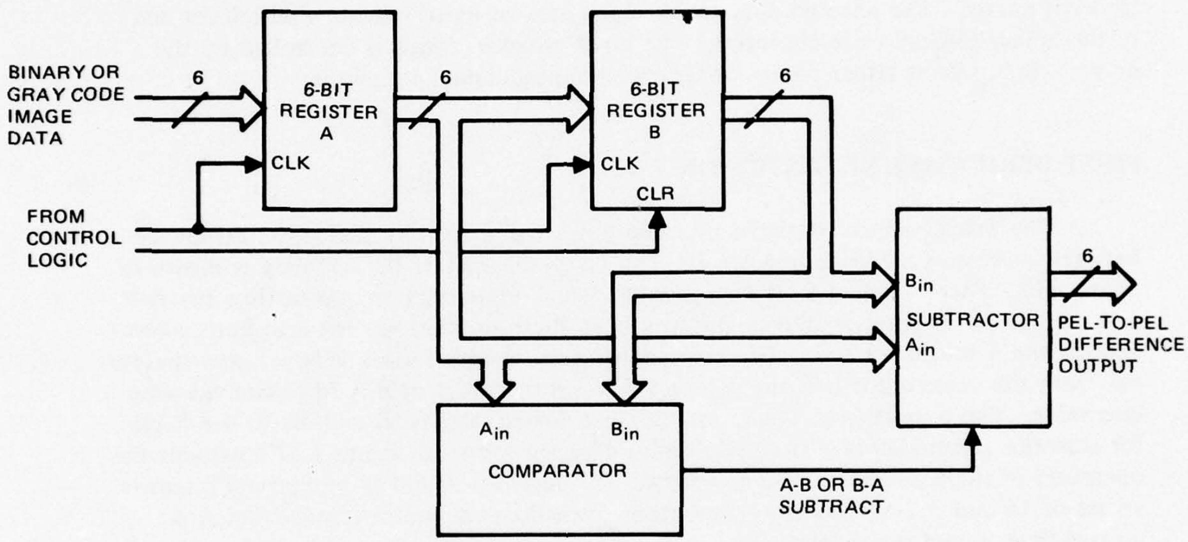


Figure A12. First derivation statistics unit.

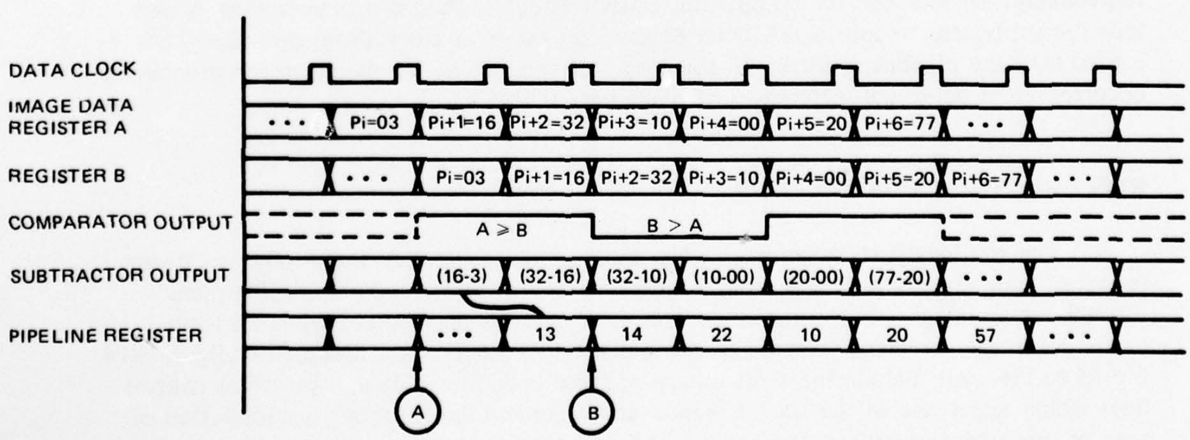


Figure A13. First derivative statistics timing diagram.

change pulse generator, which generates a pulse each time the data changes, whether it be from one to zero or zero to one. The multiplexer output is also fed into clock enable logic which enables the data change pulse onto the run length clock line at the end of the selected run. A timing diagram in figure A15 illustrates the operation of the circuit. Assuming a mode was selected to count numbers of one runs, at time interval A , the selected bit plane data output data change from zero to one, initiating a run of ones. Three clock periods later at time B the data change from one to zero. The resulting data change pulse is enabled onto the run length clock line, loading the present contents of the run length counter, which in this case is two, into the pipeline register for statistics accumulation. Note that run lengths of 1 through 64 are counted in memory locations 0 to 63, which results, in this case, in a run of length 3 being counted in memory location 2.

ADDRESS INPUT SELECTOR

The address input selector shown in figure A16 is effectively a 5:1 multiplexer which selects one of five address sources for the RAM. The first two inputs are from a Ping-Pong data register whose inputs come from the pipeline register. Statistics data coming from the pipeline register are input alternately into data register A and then data register B. The timing of these two registers will be shown later in a timing diagram. The third input to this address multiplexer is from a control counter which is used for clearing memory and for various diagnostic modes in the analyzer. The fourth address input is from a 2-digit octal lever switch on the front panel which is used for manual readout of the contents of the 64 memory locations on the LED display. The last input is from the address register in the digital controller interface. This register is used when the DIA is under program control for transfer of data from the analyzer to a digital controller.

RANDOM ACCESS MEMORY AND ARITHMETIC LOGIC UNIT

The architecture of the RAM and ALU is designed as a general-purpose digital computer central processing unit with a 24-bit data bus and 64 general-purpose accumulator/index registers. In the DIA, however, this circuitry is hardwired rather than software programmed to perform the functions required by the analyzer. A block diagram of this circuitry is shown in figure A17. The memory is a 64-word by 24-bit RAM with a 25-ns read/modify/write cycle time. The read cycle time and write cycle time are 12 ns and 18 ns, respectively. The read data register has three sources, selected by the data multiplexer, which are the RAM output, an external 24-bit data bus, and the write data register outputs. The write data register holds the output from the ALU for writing into memory. Tne ALU performs 16 arithmetic and 16 logical functions on the A and/or B data inputs. It is implemented with full lookahead carry logic to permit high-speed operation. A 24-bit addition can be performed in about 18 ns. The A input is from the read data register and the B input is currently hardwired to a plus 1 for statistics generation. The operation of these circuits and of the Ping-Pong data register, described earlier, is shown in the timing diagram in figure A18. Data output from the pipeline register and its associated data clock are the inputs to this section; phase 2 clock is generated from

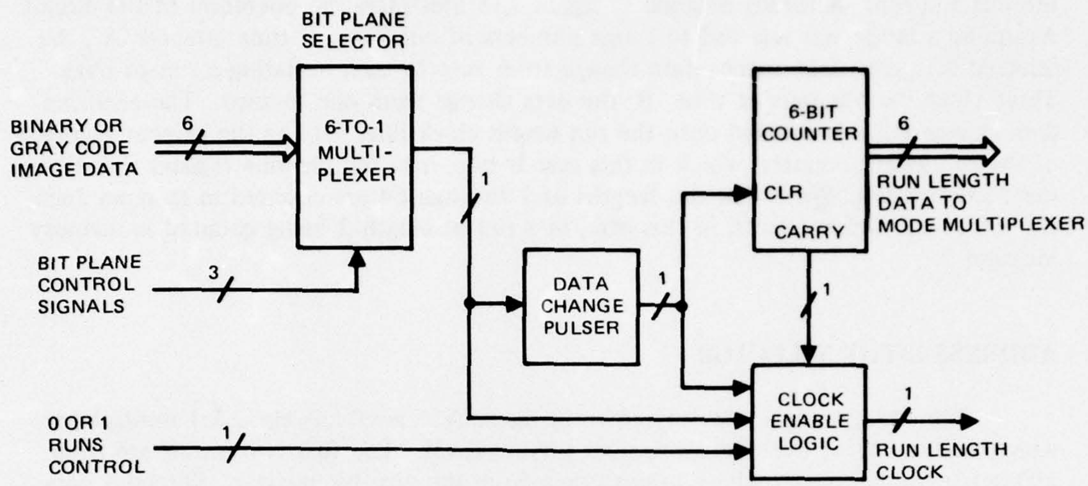


Figure A14. Run length statistics unit.

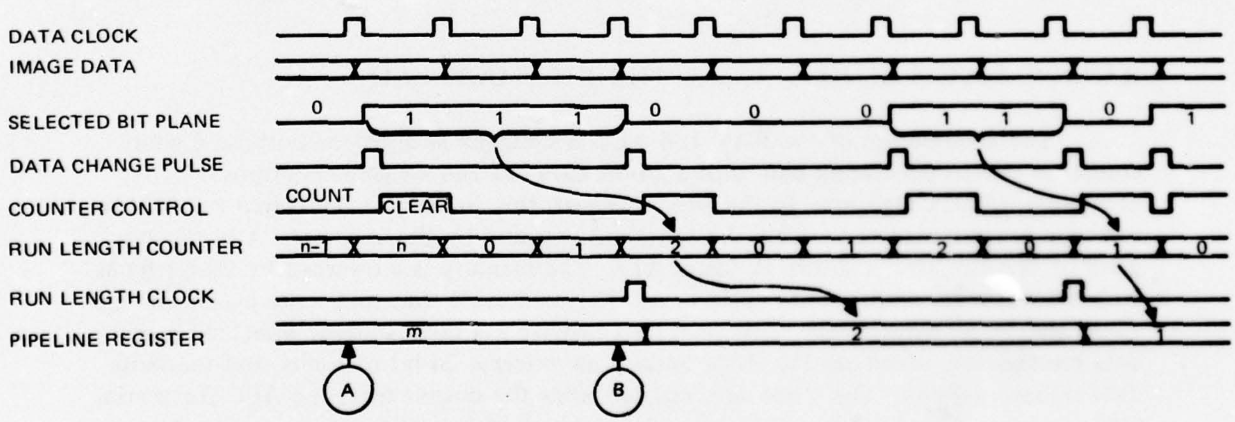
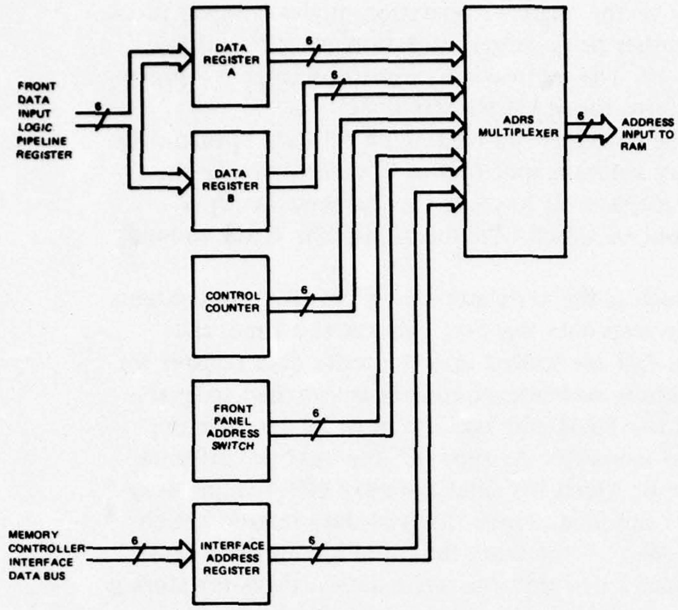


Figure A15. Run length statistics timing diagram.



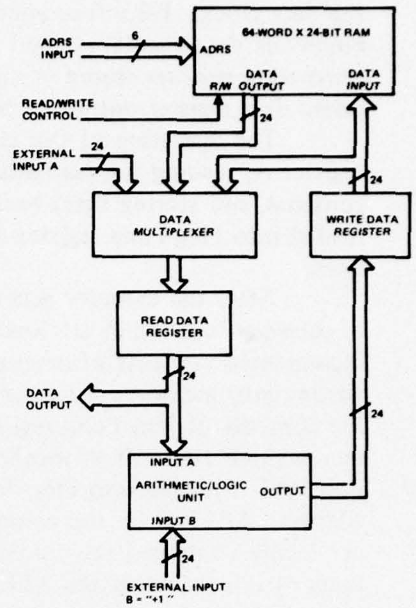


Figure A16. Address input selector.

Figure A17. RAM and ALU.

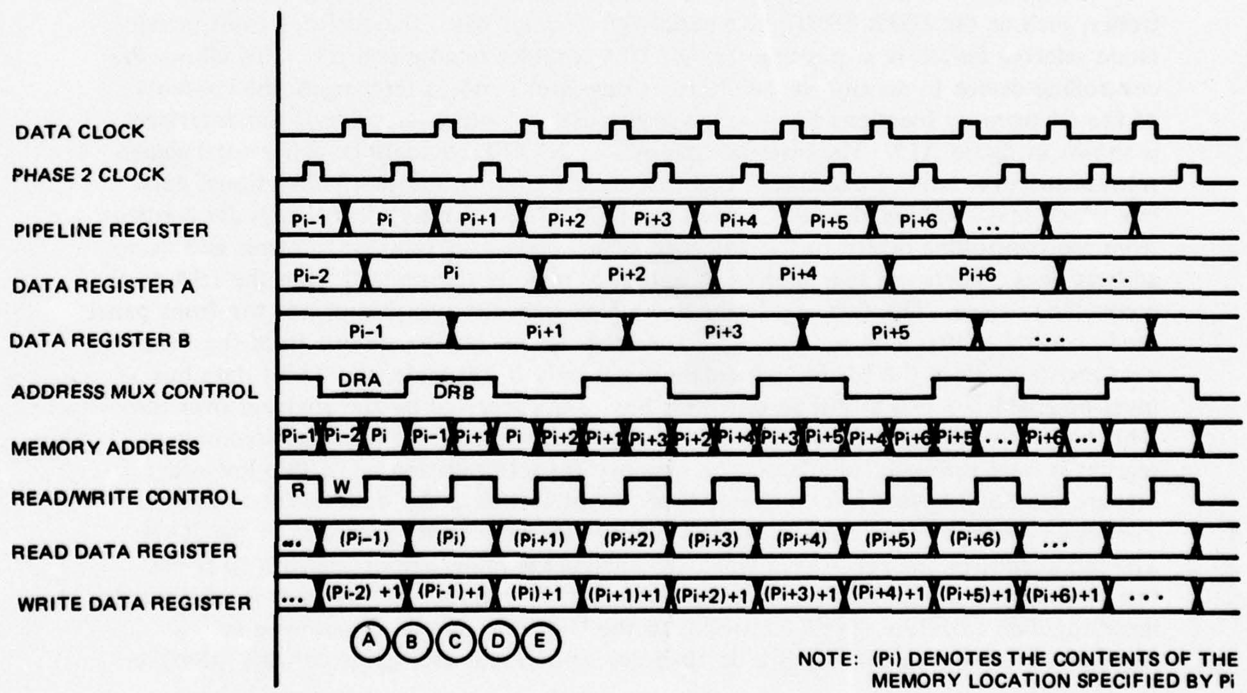


Figure A18. RAM and ALU timing diagram.

the data clock. Pel information from any of the analyzer operation modes is input to the Ping-Pong data registers A and B. Every other pel is stored in data register A and the alternating pels are stored in data register B. The address mux control selects the appropriate data register output to be enabled onto the RAM address lines.

The operation of this circuit will be described by loading of pel data P_i into data register A, reading the contents of memory location specified by P_i, incrementing the contents, and storing them back into the memory at location P_i. At time A P_i is loaded into Ping-Pong register A, the output of which is enabled onto the RAM address lines.

After the memory access time, which is the time interval A to B , the contents of memory location P_i are loaded into the read data register. Also at this time, the incremented contents of memory location P_i-1 are loaded into the write data register for writing into memory. At time B the address multiplexer control is switched to enable the contents of Ping-Pong register B onto the RAM address lines in order to write the incremented contents of location P_i-1 into memory. At time C the next pel information P_i+1 is loaded into Ping-Pong register B, which becomes the next effective memory address. At time D the contents of P_i+1 are loaded into the read data register which previously contained the contents of P_i. Also, at the same time, the incremented contents of P_i present on the ALU outputs are loaded into the write data register for storing in memory during the interval D to E , completing the processing of pel data P_i.

DIGITAL CONTROLLER INTERFACE

The digital controller interface allows the DIA to be used by any digital controller, such as the USPS FSMC, as a peripheral device. When the analyzer front panel mode selector switch is in position 77, the DIA is under remote control. This allows the controlling device to do any of the statistics operations and to interrogate the contents of the 64 memory locations for processing purposes. A block diagram of this interface is shown in figure A19. The interface consists of 13 TTL compatible, differential signals transmitted over twisted-pair lines. Eight of these signals comprise a bidirectional data bus which may transmit data to or from the DIA. The remaining five signals are controls from the controlling device to the analyzer, which consist of function controls and device address lines. There are two sources of data that may be transmitted from the DIA to the controlling device. The first is a status line which indicates whether or not the front panel mode control switch is in position 77. The other is the 24-bit data bus from the read data register. Since the bidirectional data bus is only 8 bits wide, the 24-bit data bus must be enabled 8 bits at a time onto this bus. Data received by the analyzer over the 8-bit bidirectional data bus are stored in one of three registers. The address/command register is used primarily to address the memory for interrogation. The two low-order bits are used as a byte select to enable 8 of the 24 bits onto the data bus at a time. The high-order 6 bits are used to address one of the 64 memory locations in the RAM. The mode control register is used when the analyzer is under remote control to select one of the operating modes for statistics gathering. The image data register is used when inputting data from the digital controller to the DIA for analysis. Contained in appendix A (to this appendix) is a detailed description and user guide for this interface.

BUILT-IN TEST EQUIPMENT

Incorporated in the DIA is a circuit which may be used to test the analyzer operation. A block diagram of the circuitry is shown in figure A20. It is driven by a voltage controlled oscillator with adjustable frequency whose range is approximately 10 to 25 MHz. Also included is a programmable eight-position switch which may be used to select a desired count sequence for data generation. Data are generated by a 6-bit counter which generates a binary count sequence. The variable clock rate allows testing of the analyzer at speeds up to 25 MHz.

POWER SUPPLY

The power supply for the image analyzer is a Lambda Electronics Co 5 1/4-by-19-inch rackmount unit with the following outputs.

minus 5.2 volts at 27 amperes

minus 2 volts at 9 amperes

plus 5 volts at 9 amperes

At present the power requirements for the image analyzer are:

minus 5.2 volts at 8 amperes

minus 2 volts at 5 amperes

plus 5 volts at 3 amperes

RESULTS

Presented in this section is a sample of the type of data that will be taken during the remainder of this program. To obtain the results shown here, the Video Transmission System has been used in place of the USPS scanner test bed output, since the new test bed is now under construction. The configuration of the system is shown in figure A21. A standard television camera is used to scan a page of information, the output of which is stored in the Video Transmission System frame store memory. The picture is also displayed on a CRT display associated with the Video Transmission System. Image data are then sent to the DIA for analysis. Once the statistics have been taken, the USPS FSMC is used to interrogate the DIA, transferring the information from the DIA to the FSMC for display in both tabular form on the Tektronix CRT display terminal and histogram form on the FSMC CRT display. Statistics information in tabular form may be transferred to the Tektronix hard-copy unit for hard-copy output.

Shown in figure A22 are the two samples used to demonstrate the statistics outputs. One sample of typewritten material and one sample of a continuous tone photograph were used. The television camera was set up to scan these images at a resolution which approximates the USPS requirements of 200 by 200 pels per inch. However, the television camera, with an aspect ratio of 3 to 4, cannot scan with a square resolution.

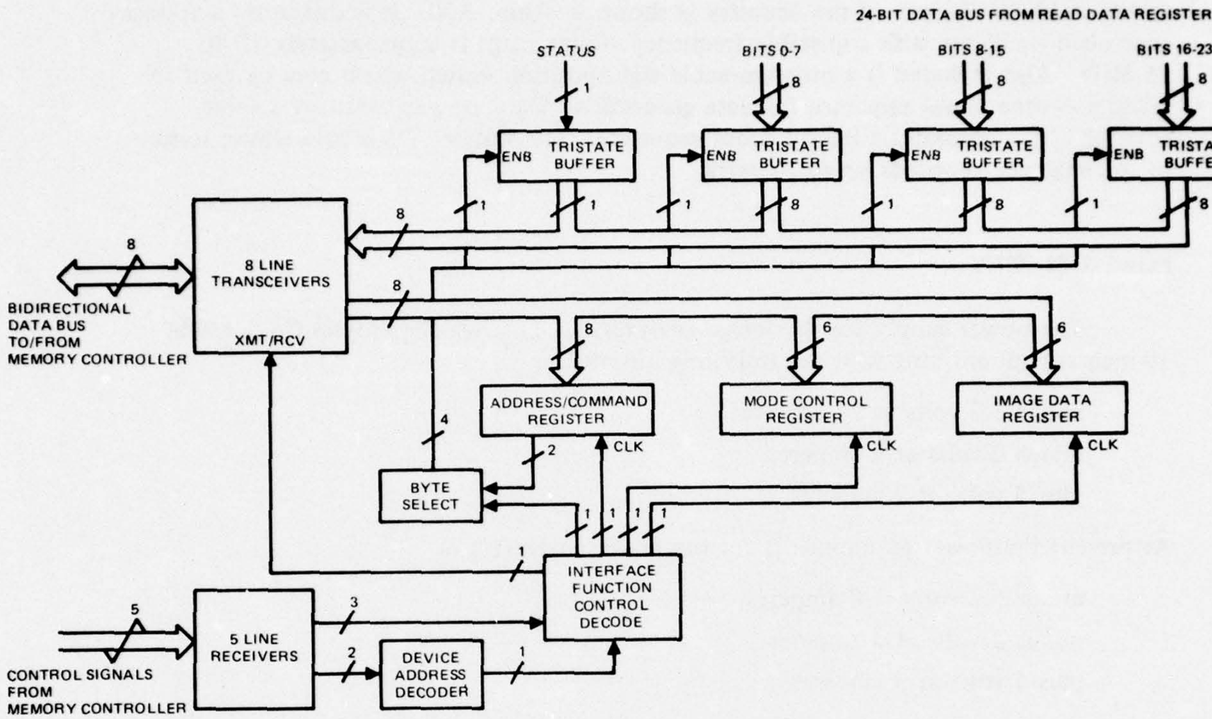


Figure A19. Digital controller interface.

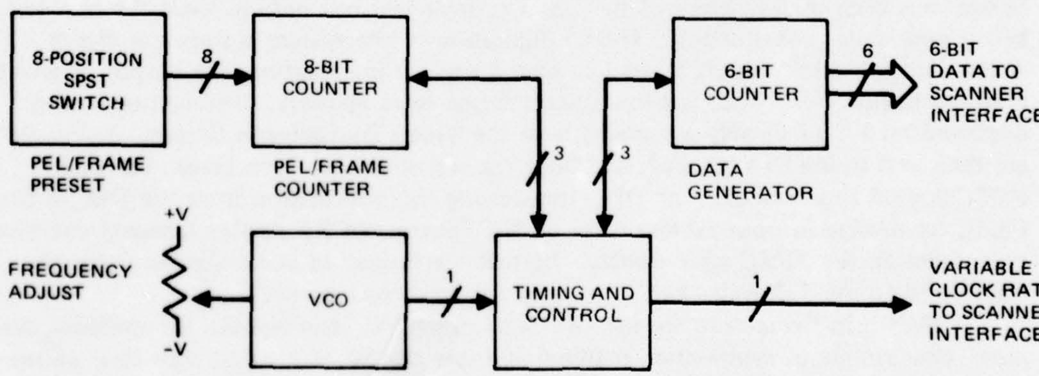


Figure A20. Built-in test equipment.

Therefore, the data presented here should be regarded as representative of data which will be taken when the new scanner test bed is completed.

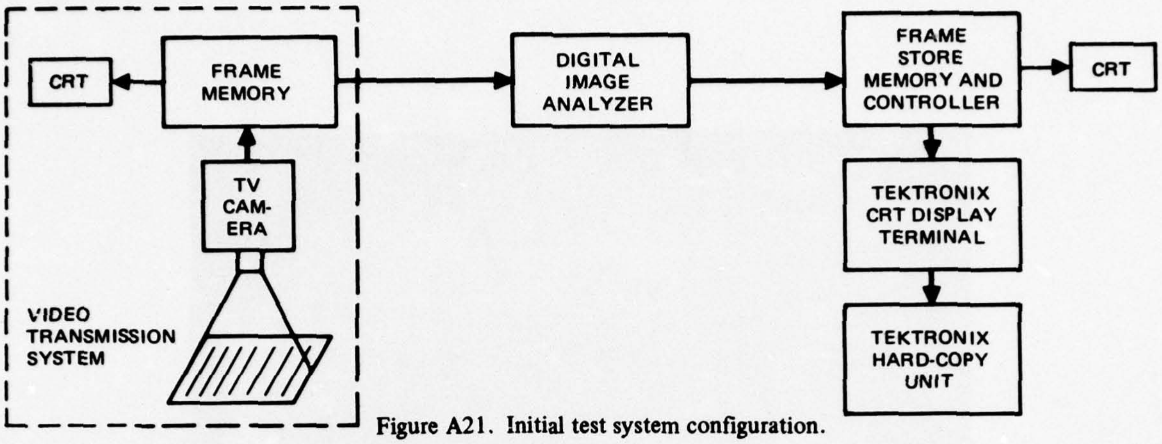


Figure A21. Initial test system configuration.

The PBS and FDS statistics are shown in figure A23 for the two samples. From the PBS statistics it can be seen that the general trend is in agreement with the idealized figure presented in the Prescanner Image Analysis section.

The PBS statistics for the two images show the general differences expected for typewritten material versus continuous tone picture information. The first derivative statistics, however, are almost identical for the two pictures. These statistics in tabular form output from the Tektronix hard-copy unit are presented in appendix B (to this appendix).

Figures A24 and A25 show the RLS histograms for the two samples. In each figure the histograms represent the total number of zero runs occurring in the images in all six bit planes. The data in tabular form are contained in appendix B. As can be seen in these histograms, there is a periodicity that is yet unexplained. It appears that at every fourth location there is a much larger number than in the rest, indicating that most zero runs occur with lengths of 1, 5, 9, 13, etc. The cause of this abnormality will be resolved in the next report.

The DIA has been tested in operation using the built-in test equipment and has been determined to operate up to a maximum of 20.4 MHz, closely approaching the design goal of 21 MHz. The interfaces from the DIA to the FSMC, to the scanner test bed, and to the Video Transmission System all operate satisfactorily.

CONCLUSIONS AND SUMMARY

The image analyzer is operating in all performance modes as planned. The modes available include:

- Pel Brightness Statistics (PBS)
- First Derivative Statistics (FDS)
- Run Length Statistics (RLS)

  Binary of Gray code

  One of six bit planes selectable

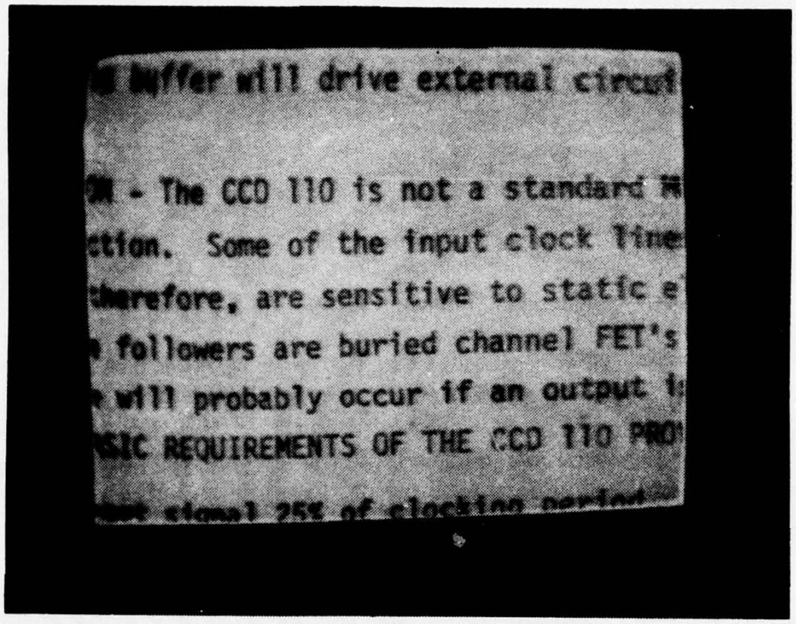
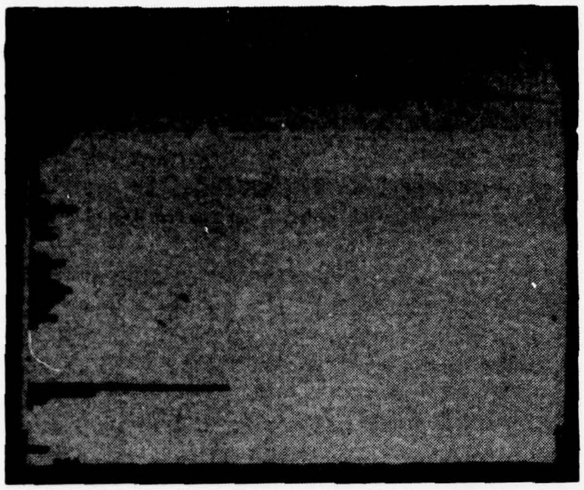
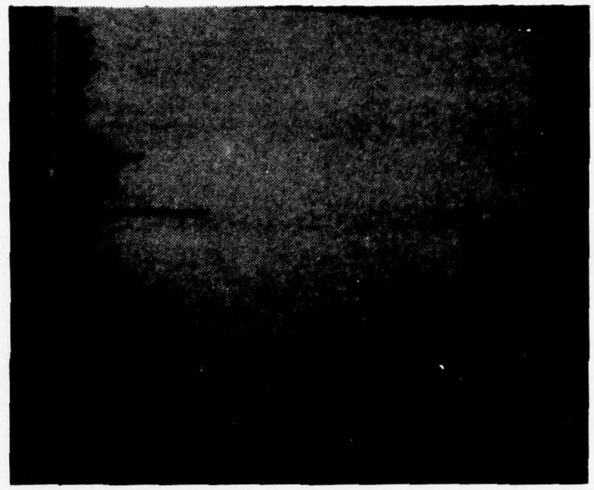


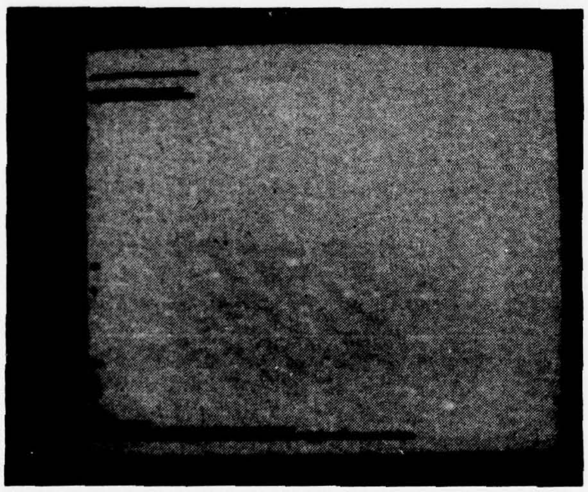
Figure A 22. Sample typewritten and continuous tone images.



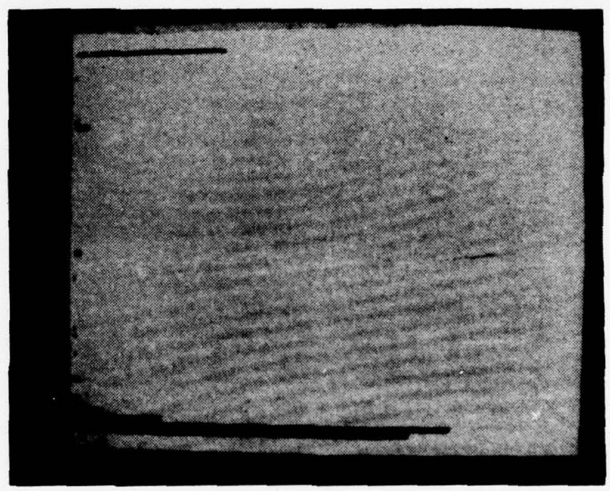
PEL BRIGHTNESS STATISTICS



PEL BRIGHTNESS STATISTICS



FIRST DERIVATIVE STATISTICS

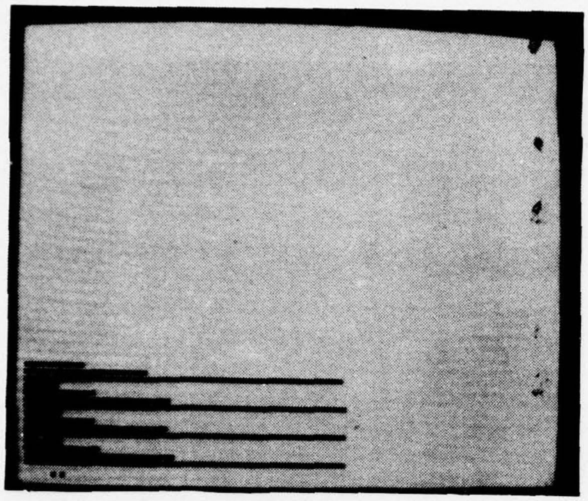


FIRST DERIVATIVE STATISTICS

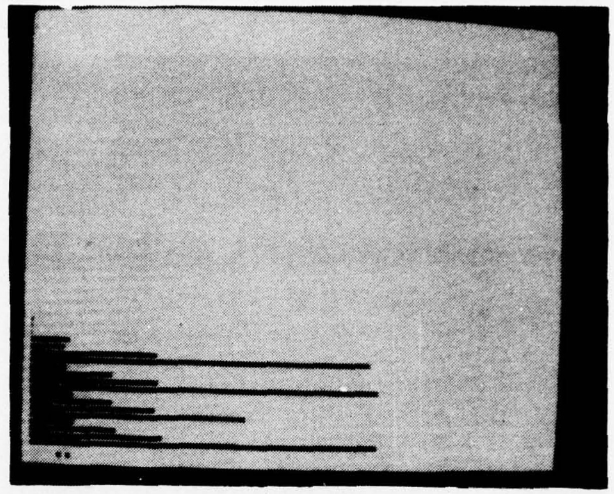
TYPEWRITTEN SAMPLE 1

CONTINUOUS TONE SAMPLE 2

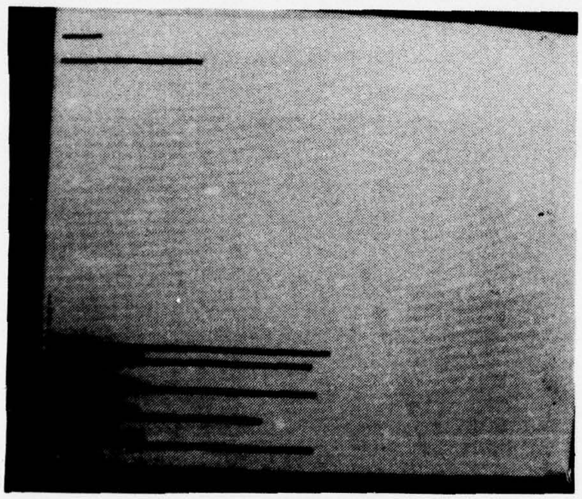
Figure A23. PBS and FDS statistics.



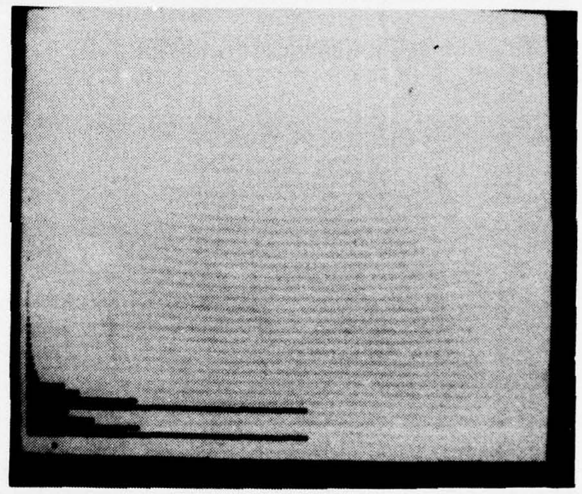
BIT PLANE 1



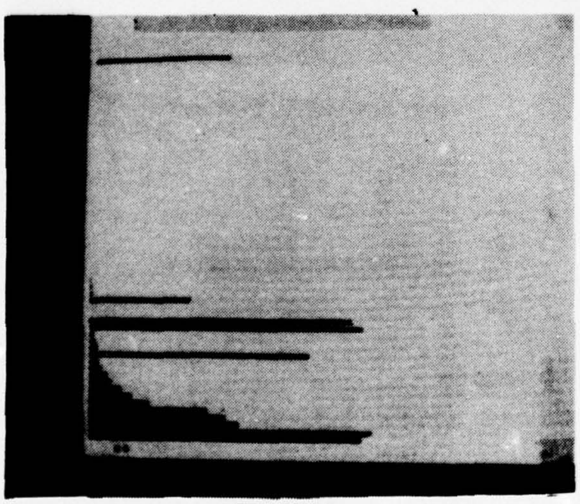
BIT PLANE 2



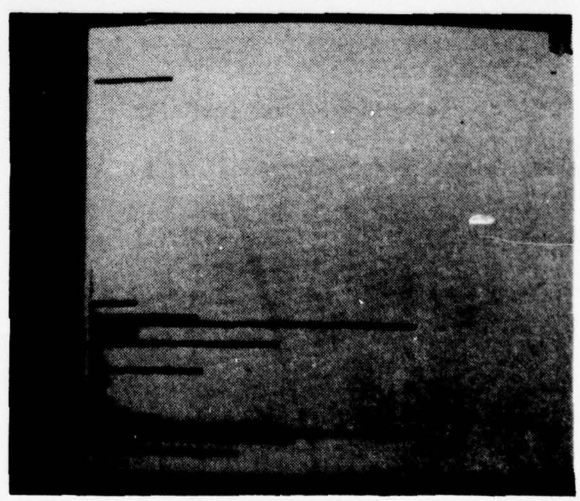
BIT PLANE 3



BIT PLANE 4

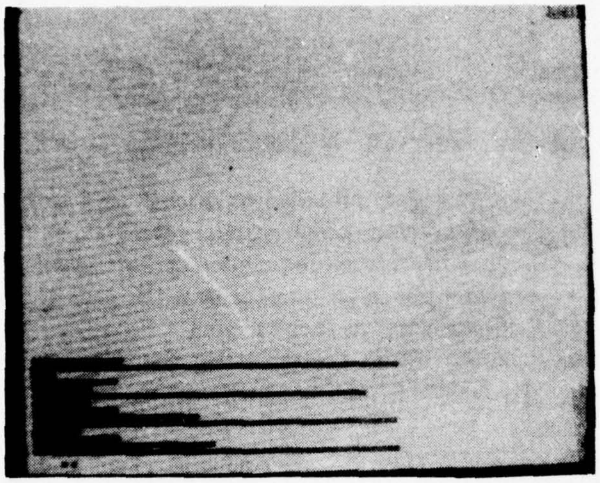


BIT PLANE 5

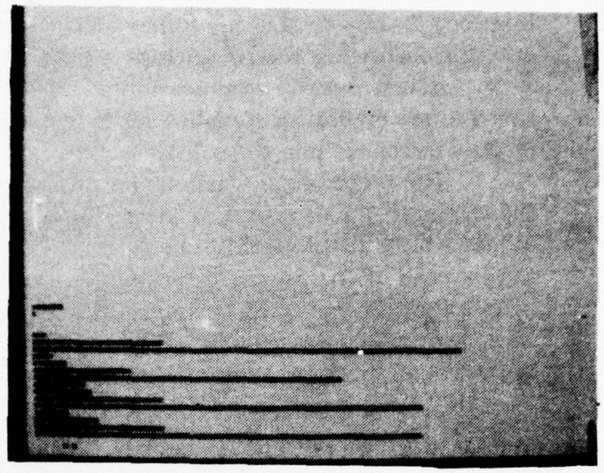


BIT PLANE 6

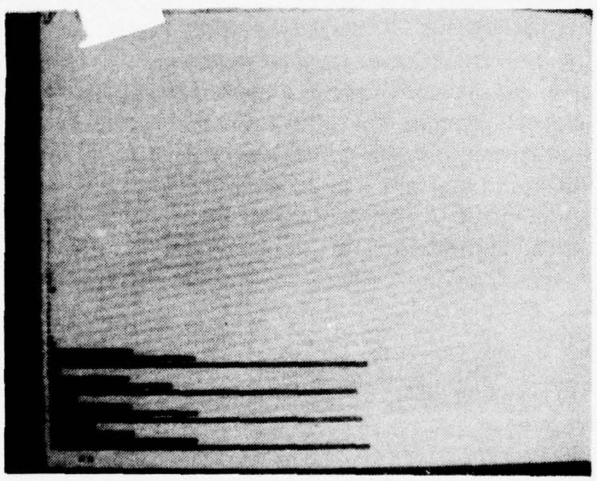
Figure A24. Run length statistics, typewritten sample 1.



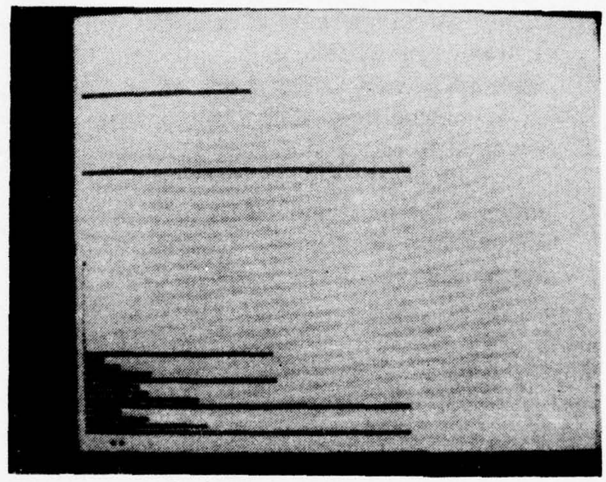
BIT PLANE 1



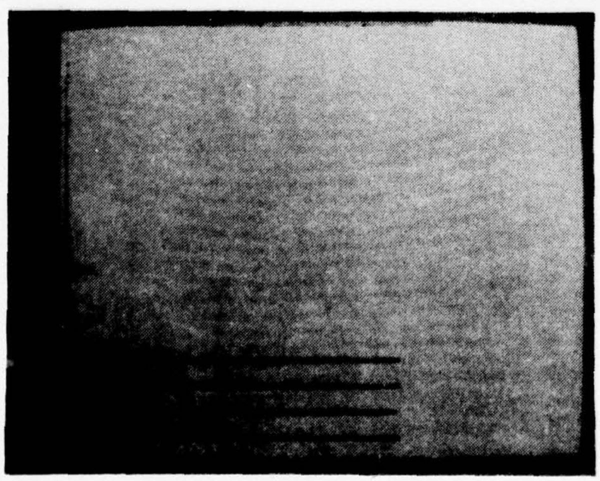
BIT PLANE 2



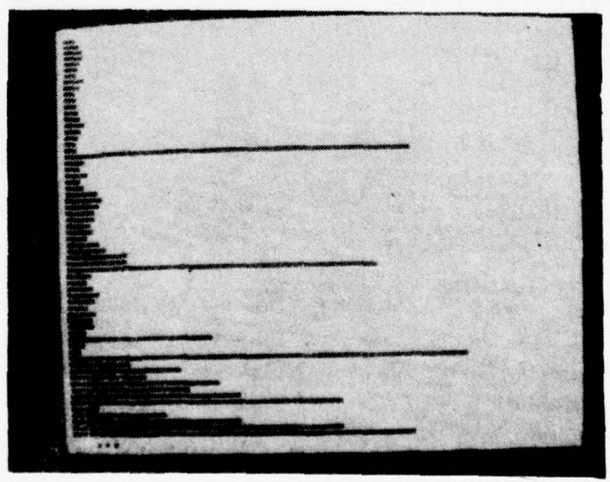
BIT PLANE 3



BIT PLANE 4



BIT PLANE 5



BIT PLANE 6

Figure A25. Run length statistics, continuous tone sample 2.

The analyzer is compatible with two interfaces. The high-speed data input port can accept 6-bit pel data words at a rate of 20.4 megapels per second. A general-purpose digital controller interface allows analyzer operation as a peripheral device. Through this interface devices such as the Frame Store Memory Controller can either transmit image data for analysis or receive analysis results for processing and display.

A very cursory examination of the first system results from the analyzer indicates that the pel brightness statistics are in agreement with the ideal image model discussed in the Prescanner Image Analysis section.

The preceding discussions on prescanner image analysis were provided to orient the reader to the direction of the pending research. The supporting computational techniques will be developed during the next reporting period. It should be remembered that the purpose of the proposed techniques presented is to reduce the total number of bits of information that must be transmitted to present the information at the receiving station in satisfactory quality. The techniques being explored will in no way affect the types of compression coding which can be applied to the resulting data.

PLANNED FUTURE NELC ACTIVITIES

A complete set of statistics will be generated for a group of images including typewritten, handwritten, and continuous tone photographs. These images will be scanned with a Fairchild CCD121 imager, digitized, and stored on magnetic tape for the analyses.

Using these statistics, a development will begin to generate the various algorithms required to set up the main scanner controls in an electronic message input terminal.

If a need for the high data rate appears to exist, an attempt will be made to increase the maximum operating speed of the image analyzer to the design goal of 21 megapels per second. This will be dependent on the architecture of the new RCA tracking imager device.

APPENDIX A (TO TR 2020 APPENDIX A): DIGITAL CONTROLLER INTERFACE DESCRIPTION

INTRODUCTION

This is a description of that portion of the Digital Image Analyzer (DIA) which allows a general-purpose digital controller such as the USPS Frame Store Memory Controller (FSMC) to use the DIA as a peripheral device.

All numerical constants used are in octal notation unless otherwise specified.

INTERFACE CONNECTOR AND SIGNAL DESCRIPTION

There are 13 TTL differential, twisted-pair signal lines comprising this interface. Eight of these are a bidirectional data bus, four are control lines, and one is a strobe line. They are defined by connector pin number, signal name, and function, as follows:

Connector Pin +	Connector Pin −	Signal Name		
P01	P14	BDB0	(LSB)	8-bit bidirectional data bus
P02	P15	BDB1		
P03	P16	BDB2		
P04	P17	BDB3		
P05	P18	BDB4		
P06	P19	BDB5		
P07	P20	BDB6		
P08	P21	BDB7	(MSB)	
P09	P22	DA0	(LSB)	Device to DIA
P10	P23	DA1	(MSB)	
P11	P24	FC0	(LSB)	Interface function control to DIA
P12	P25	FC1	(MSB)	
P13	P26	STB		Strobe to DIA

BIDIRECTIONAL DATA BUS BDB7 - BDB0

Data transmitted from the digital controller to the DIA consist of either RAM address, mode, command, or image information, depending on the Function Control code FC1-FC0. Data transmitted from the DIA to the digital controller will consist of either image statistics information or the front panel mode switch setting.

DEVICE ADDRESS DA1 - DA0

The DIA device address is DA1-DA0=01. This code must be present on these lines for every I/O transfer to or from the analyzer.

FUNCTION CONTROL FC1 - FC0

The four possible Function Control codes are described as follows:

FC1=FC0	Function
00	This code enables the Strobe to clock an 8-bit word into the DIA Address Register (AR) as received from the digital controller.
01	This code enables the Strobe to clock an 8-bit word into the analyzer Mode Control Register (MCR).
02	This code enables the Strobe to clock a 6-bit word (BDB5-BDB0) into the DIA Image Input Register (IIR)
03	This code enables an 8-bit byte of data onto the Bidirectional Data Bus for transmission to the digital controller. The digital controller must disable the transmitters on the Bidirectional Data Bus before this Function Code is transmitted to the DIA to prevent bus contention.

STROBE STB

This Strobe is used to clock data into the various registers in the digital controller interface.

INTERFACE REGISTER DESCRIPTION

Address Register AR7-AR0

MSB LSB

$$\underbrace{7 \quad 6 \quad 5 \quad 4 \quad 3 \quad 2}_{\text{Address/Command Select}} \qquad \underbrace{1 \quad 0}_{\text{Byte/Control Select}}$$

The primary purpose of this register is to address one of three 8-bit bytes in one of the 64 (decimal) words of the RAM in the DIA for interrogation by the digital controller. This register is also used to generate various commands to the analyzer and to interrogate the analyzer front panel mode control switch setting.

The Byte/Control Select bits determine which of these functions is to be performed in the following manner:

AR1-AR0	Function
00	Selects command mode and allows interrogation of the front panel mode control switch setting. The analyzer commands are decoded as follows, using bits AR7-AR2 of the Address Register:

AR7-AR2	Function
00	NOP - no operation.
01	Data Available - must be set while image data are being transmitted to the DIA by a digital controller for analysis.
02	Master Reset - also clears the Address Register.
03	Execute - used to initiate certain modes of analyzer operation. Modes requiring the Execute command are described in the Mode Control Register section. Address Register must be cleared (or contents changed) between sucessive Execute commands.
04-77	Not used.

For interrogation of the front panel mode control switch setting, the Function Control lines must be FC1-FC0=03. A 1-bit code is then enabled onto the Bidirectional Data Bus line BDB0. This code is "1" if 77 is entered via the switch and "0" for all other switch settings. This setting, 77 is required for the DIA to receive commands from or transmit data to the digital controller. Here, AR7-AR2 are "don't care."

01	When FC1-FC0=03, the most significant 8-bit byte of the 24-bit memory word addressed by bits AR7-AR2 is enabled onto the Bidirectional Data Bus for transmission to the digital controller.
02	When FC1-FC0=03, the middile 8-bit byte of the 24-bit memory word addressed by bits AR7-AR2 is enabled onto the Bidirectional Data Bus for transmission to the digital controller.

MODE CONTROL REGISTER MCR7-MCR0

Before image data are transmitted to the DIA for analysis, the Mode Control Register (MCR) must be loaded with the appropriate code for the desired analysis mode. The operating modes for the DIA are as follows:

MCR7-MCR0	Mode Description
00	PBS Binary.
01	RLS Binary 0-runs BP-1 (LSB)
02	RLS Binary 0-runs BP-2
03	RLS Binary 0-runs BP-3
04	RLS Binary 0-runs BP-4
05	RLS Binary 0-runs BP-5
06	RLS Binary 0-runs BP-6 (MSB)
07	FDS
10	PBS Binary Subtract mode
11	RLS Binary 1-runs BP-1
12	RLS Binary 1-runs BP-2
13	RLS Binary 1-runs BP-3
14	RLS Binary 1-runs BP-4
15	RLS Binary 1-runs BP-5
16	RLS Binary 1-runs BP-6
17	Not used
20	PBS Gray Code
21	RLS Gray Code 0-runs BP-1
22	RLS Gray Code 0-runs BP-2

MCR7-MCR0	Mode Description
23	RLS Gray Code 0-runs BP-3
24	RLS Gray Code 0-runs BP-4
25	RLS Gray Code 0-runs BP-5
26	RLS Gray Code 0-runs BP-6
27	FDS
30	PBS Gray Code Subtract mode
31	RLS Gray Code 1-runs BP-1
32	RLS Gray Code 1-runs BP-2
33	RLS Gray Code 1-runs BP-3
34	RLS Gray Code 1-runs BP-4
35	RLS Gray Code 1-runs BP-5
36	RLS Gray Code 1-runs BP-6
37	Not used
40	Read contents of 24-bit word of RAM addressed by AR7-AR2. LED display is enabled by this code.
41	Clear all 64 words of RAM. Execute command needed.
42	Store contents of external, manually switched data bus in memory location selected by AR7-AR2. Execute command needed.
43	Store contents of external, manually switched data bus in all memory locations. Execute command needed.
44	Continuous increment of contents of memory location selected by AR7-AR2. Execute command needed to start. Master reset command needed to stop.
45	Continuous decrement of contents of memory location selected by AR7-AR2. Execute command needed to start. Master reset command needed to stop.
46-77	Not used.

IMAGE INPUT REGISTER V7-V0

The Image Input Register is used to input binary image information to the DIA for analysis.

APPENDIX B (TO TR 2020 APPENDIX A):

IMAGE ANALYSIS RESULTS IN TABULAR FORM

Typewritten Sample #1
PEL Brightness Statistics

L	#	L	#	L	#	L	#
0	124096	16	9984	32	115840	48	344640
1	896	17	12032	33	41856	49	554944
2	640	18	51264	34	128704	50	1066496
3	1344	19	170880	35	269952	51	1702208
4	1920	20	98880	36	110144	52	2297408
5	5760	21	139840	37	33600	53	3170880
6	27840	22	206272	38	83840	54	2938496
7	112000	23	246144	39	23680	55	2672128
8	388032	24	169664	40	39872	56	2630848
9	1182208	25	115584	41	45504	57	1921216
10	9536	26	111424	42	32704	58	1005568
11	7744	27	210368	43	96832	59	246976
12	5824	28	109760	44	159232	60	7680
13	13568	29	25600	45	203136	61	25344
14	5760	30	23040	46	212096	62	22144
15	7424	31	155712	47	[illegible]	63	[illegible]

Typewritten Sample #1
First Derivative Statistics

L	#	L	#	L	#	L	#
0	472184	16	1026	32	264	48	548
1	286850	17	388	33	184	49	222
2	78908	18	216	34	48	50	16
3	29788	19	178	35	84	51	64
4	17072	20	162	36	46	52	34
5	9132	21	174	37	28	53	26
6	5144	22	240	38	18	54	36
7	9022	23	186	39	154	55	356
8	11994	24	7078	40	26	56	147232
9	5490	25	190	41	40	57	131304
10	3552	26	140	42	8	58	158
11	2398	27	110	43	12	59	406
12	16386	28	9806	44	46	60	153226
13	718	29	148	45	38	61	2
14	654	30	440	46	14	62	0
15	174	31	74	47	66	63	348

Typewritten Sample #1
Run Length Statistics 0-Runs Bit Plane 1

L	#	L	#	L	#	L	#
0	227024	16	4	32	0	48	0
1	101952	17	8	33	0	49	0
2	50940	18	4	34	0	50	0
3	25760	19	4	35	0	51	0
4	226732	20	12	36	0	52	0
5	97096	21	4	37	0	53	0
6	47516	22	0	38	0	54	0
7	25580	23	0	39	0	55	0
8	227032	24	0	40	0	56	0
9	99948	25	0	41	0	57	0
10	47944	26	0	42	0	58	0
11	24096	27	0	43	0	59	0
12	224856	28	0	44	0	60	0
13	84004	29	0	45	0	61	0
14	40712	30	0	46	0	62	0
15	120	31	0	47	0	63	0

Typewritten Sample #1
Run Length Statistics 0-Runs Bit Plane 2

L	#	L	#	L	#	L	#
0	152888	16	556	32	160	48	4
1	55760	17	896	33	152	49	8
2	35916	18	1128	34	56	50	8
3	18216	19	440	35	144	51	0
4	91688	20	344	36	20	52	0
5	52620	21	236	37	32	53	0
6	34328	22	272	38	24	54	4
7	18116	23	200	39	20	55	0
8	152892	24	120	40	12	56	4
9	53672	25	108	41	12	57	4
10	34292	26	76	42	4	58	4
11	14964	27	92	43	16	59	0
12	149268	28	88	44	4	60	0
13	53200	29	60	45	16	61	0
14	14420	30	76	46	0	62	8
15	16744	31	60	47	0	63	0

Typewritten Sample #1
Run Length Statistics 0-Runs Bit Plane 4

L	#	L	#	L	#	L	#
0	27136	16	350	32	68	48	26
1	10568	17	234	33	50	49	30
2	6296	18	158	34	74	50	24
3	3876	19	168	35	110	51	20
4	26846	20	160	36	78	52	14
5	10324	21	116	37	44	53	18
6	4910	22	120	38	60	54	20
7	3486	23	84	39	44	55	26
8	1094	24	88	40	62	56	32
9	974	25	88	41	46	57	34
10	782	26	112	42	34	58	20
11	628	27	82	43	46	59	18
12	446	28	82	44	52	60	36
13	398	29	90	45	54	61	30
14	338	30	76	46	34	62	32
15	318	31	82	47	50	63	16

Typewritten Sample #1
Run Length Statistics 0-Runs Bit Plane 3

L	#	L	#	L	#	L	#
0	86564	16	492	32	144	48	60
1	30656	17	384	33	288	49	56
2	20916	18	988	34	168	50	56
3	12168	19	1020	35	112	51	56
4	68232	20	600	36	96	52	48
5	29032	21	512	37	128	53	44
6	19828	22	292	38	108	54	32
7	11732	23	260	39	80	55	68
8	86564	24	236	40	96	56	44984
9	28532	25	196	41	92	57	72
10	20048	26	276	42	108	58	56
11	7056	27	212	43	76	59	320
12	85048	28	156	44	88	60	12680
13	30136	29	184	45	84	61	28
14	90972	30	152	46	48	62	60
15	15740	31	128	47	64	63	56

Typewritten Sample #1
Run Length Statistics 0-Runs Bit Plane 5

L	#	L	#	L	#	L	#
0	12012	16	12012	32	8	48	4
1	12480	17	11540	33	12	49	4
2	6432	18	12	34	8	50	8
3	5852	19	12	35	4	51	0
4	5080	20	4376	36	4	52	8
5	2572	21	140	37	4	53	0
6	1812	22	116	38	4	54	0
7	1384	23	56	39	4	55	0
8	948	24	28	40	0	56	5932
9	772	25	28	41	0	57	8
10	552	26	32	42	4	58	0
11	380	27	32	43	0	59	4
12	9556	28	16	44	4	60	0
13	360	29	12	45	4	61	0
14	236	30	16	46	0	62	0
15	164	31	8	47	0	63	0

Typewritten Sample #1
Run Length Statistics 0-Runs Bit Plane 6

L	#	L	#	L	#	L	#
0	3132	16	3972	32	8	48	0
1	956	17	956	33	8	49	4
2	4328	18	1008	34	4	50	0
3	7252	19	7028	35	4	51	0
4	4012	20	2264	36	4	52	4
5	1420	21	68	37	4	53	0
6	808	22	992	38	4	54	0
7	472	23	36	39	0	55	0
8	360	24	64	40	4	56	1672
9	264	25	56	41	0	57	4
10	344	26	28	42	4	58	0
11	336	27	24	43	0	59	4
12	2384	28	16	44	0	60	0
13	364	29	12	45	0	61	0
14	264	30	12	46	0	62	0
15	240	31	8	47	0	63	0

Continuous Tone Sample #2
PEL Brightness Statistics

L	#	L	#	L	#	L	#
0	378	16	13056	32	3954	48	4334
1	16840	17	11295	33	4182	49	2867
2	9526	18	10739	34	6088	50	2618
3	371	19	9129	35	6037	51	4675
4	412	20	8322	36	5191	52	2823
5	5693	21	7655	37	6569	53	2909
6	35949	22	7346	38	6641	54	4080
7	38911	23	5568	39	7274	55	2145
8	17681	24	7173	40	7576	56	3832
9	9999	25	3844	41	6307	57	4133
10	8519	26	4766	42	5182	58	2881
11	7865	27	4506	43	3478	59	4927
12	6727	28	3211	44	2996	60	2555
13	7049	29	4383	45	2965	61	3304
14	12707	30	4606	46	2726	62	1849
15	14557	31	14458	47	1952	63	3019

Continuous Tone Samle #2
First Derivative Statistics

L	#	L	#	L	#	L	#
0	152252	16	613	32	362	48	6143
1	171086	17	158	33	113	49	1017
2	37455	18	68	34	5	50	8
3	11844	19	60	35	51	51	15
4	4928	20	68	36	4	52	3
5	1581	21	72	37	2	53	5
6	121	22	56	38	4	54	3
7	141	23	50	39	106	55	20
8	2186	24	469	40	8	56	539
9	369	25	54	41	4	57	96
10	118	26	37	42	4	58	37
11	229	27	47	43	3	59	252
12	781	28	2713	44	9	60	65803
13	342	29	59	45	39	61	72
14	210	30	76	46	2	62	66
15	474	31	48	47	159	63	343

Continuous Tone Sample #2
Run Length Statistics 0-Runs Bit Plane 1

L	#	L	#	L	#	L	#
0	55237	16	22	32	2	48	0
1	26055	17	24	33	0	49	0
2	12475	18	23	34	0	50	0
3	6702	19	7	35	0	51	0
4	54739	20	37	36	1	52	0
5	23796	21	5	37	0	53	0
6	12302	22	6	38	0	54	0
7	7679	23	2	39	0	55	0
8	50813	24	2	40	0	56	0
9	8566	25	4	41	1	57	0
10	12241	26	3	42	0	58	0
11	3611	27	5	43	0	59	0
12	54928	28	2	44	0	60	0
13	3187	29	0	45	0	61	0
14	55	30	4	46	0	62	0
15	45	31	0	47	0	63	0

Continuous Tone Sample #2
Run Length Statistics 0-Runs Bit Plane 2

L	#	L	#	L	#	L	#
0	51479	16	120	32	6	48	0
1	16306	17	70	33	6	49	3
2	8222	18	4154	34	13	50	1
3	4437	19	74	35	3	51	1
4	51445	20	35	36	5	52	2
5	16116	21	67	37	9	53	0
6	8095	22	62	38	2	54	2
7	7645	23	30	39	3	55	3
8	39445	24	30	40	10	56	1
9	12403	25	36	41	1	57	1
10	4354	26	18	42	0	58	2
11	2406	27	12	43	5	59	1
12	54135	28	29	44	3	60	0
13	16306	29	10	45	2	61	0
14	1838	30	13	46	3	62	1
15	138	31	22	47	0	63	0

Continuous Tone Sample #2
Run Length Statistics 0-Runs Bit Plane 3

L	#	L	#	L	#	L	#
0	24166	16	129	32	40	48	18
1	8915	17	99	33	31	49	6
2	4661	18	115	34	38	50	13
3	2689	19	108	35	29	51	15
4	24129	20	85	36	44	52	12026
5	8368	21	149	37	33	53	22
6	4632	22	68	38	25	54	13
7	4057	23	140	39	27	55	8
8	13684	24	124	40	24166	56	23
9	4982	25	85	41	33	57	7
10	2622	26	255	42	23	58	7
11	1543	27	62	43	23	59	7
12	13444	28	54	44	23	60	8
13	210	29	67	45	10	61	9
14	175	30	50	46	27	62	8
15	161	31	43	47	17	63	10

Continuous Tone Sample #2
Run Length Statistics 0-Runs Bit Plane 4

L	#	L	#	L	#	L	#
0	14717	16	209	32	54	48	20
1	6516	17	139	33	59	49	28
2	3754	18	116	34	50	50	24
3	1941	19	148	35	42	51	22
4	14308	20	111	36	48	52	39
5	6508	21	102	37	48	53	22
6	3574	22	92	38	41	54	25
7	1193	23	405	39	48	55	33
8	14024	24	121	40	44	56	29
9	5401	25	106	41	34	57	38
10	3532	26	84	42	49	58	37
11	417	27	71	43	11	59	15
12	14572	28	84	44	29	60	26
13	6471	29	66	45	27	61	21
14	3739	30	68	46	31	62	24
15	308	31	69	47	20	63	19

Continuous Tone Sample #2
Run Length Statistics 0-Runs Bit Plane 5

L	#	L	#	L	#	L	#
0	4992	16	83	32	45	48	37
1	1811	17	74	33	46	49	34
2	1065	18	76	34	45	50	39
3	527	19	76	35	54	51	40
4	4952	20	65	36	38	52	38
5	39	21	53	37	36	53	29
6	896	22	66	38	46	54	23
7	308	23	58	39	40	55	38
8	4976	24	72	40	30	56	49
9	1398	25	63	41	37	57	47
10	49	26	403	42	33	58	30
11	47	27	93	43	41	59	47
12	4986	28	50	44	31	60	20
13	1481	29	51	45	30	61	21
14	880	30	39	46	40	62	28
15	165	31	46	47	44	63	28

Continuous Tone Sample #2
Run Length Statistics 0-Runs Bit Plane 6

L	#	L	#	L	#	L	#
0	427	16	23	32	33	48	20
1	335	17	33	33	31	49	26
2	205	18	32	34	36	50	21
3	115	19	36	35	35	51	18
4	34	20	25	36	42	52	17
5	335	21	34	37	46	53	15
6	205	22	41	38	39	54	14
7	145	23	33	39	23	55	20
8	182	24	26	40	19	56	26
9	93	25	30	41	28	57	16
10	135	26	383	42	19	58	17
11	74	27	73	43	26	59	19
12	496	28	74	44	427	60	23
13	16	29	48	45	16	61	23
14	20	30	40	46	16	62	21
15	174	31	25	47	18	63	16

APPENDIX B: FRAME STORE MEMORY AND DISPLAY

Prepared

for

US POSTAL SERVICE

May 1976

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INTRODUCTION

The USPS image acquisition system requires a document scanner section which includes the paper handler, the electronic imager, the illumination source, and the optics assembly. The output from the acquisition system exists in the form of high-speed, sampled-data electrical signals. The video output rate is 84 megasamples per second. This rate can be divided into four data streams at 21 megasamples per second, or eight data streams at 10.5 megasamples per second each. The data stream or streams at this point are electrically preprocessed, if desired, and are converted to digital equivalents for each sample (see fig B1).

The information at this point is both volatile and sequential. The serial streams of image samples emerge one after another as the scanners discharge the results of acquiring a single line of optical data. This is true whether the imager is a line imager or an area imager. Once the streams are discharged, the image acquisition and electrical pre-processing subsystems have no access to adjacent samples for further processing, manipulation, or retiming for transmission unless there is memory.

Some small "scratch pad" memory, even as much as two to four lines of image data (1800 to 7200 pels by 6 bits) may be contained in the preprocessor circuitry and the prescan image analyzer. However, for significant memory capacity to perform not only developmental investigations but actual on-line image acquisition and transmission, a large "frame store" memory will be required.

This report describes the architecture and capabilities of an experimental frame store memory and its associated memory controller developed at NELC for Postal Service investigations.

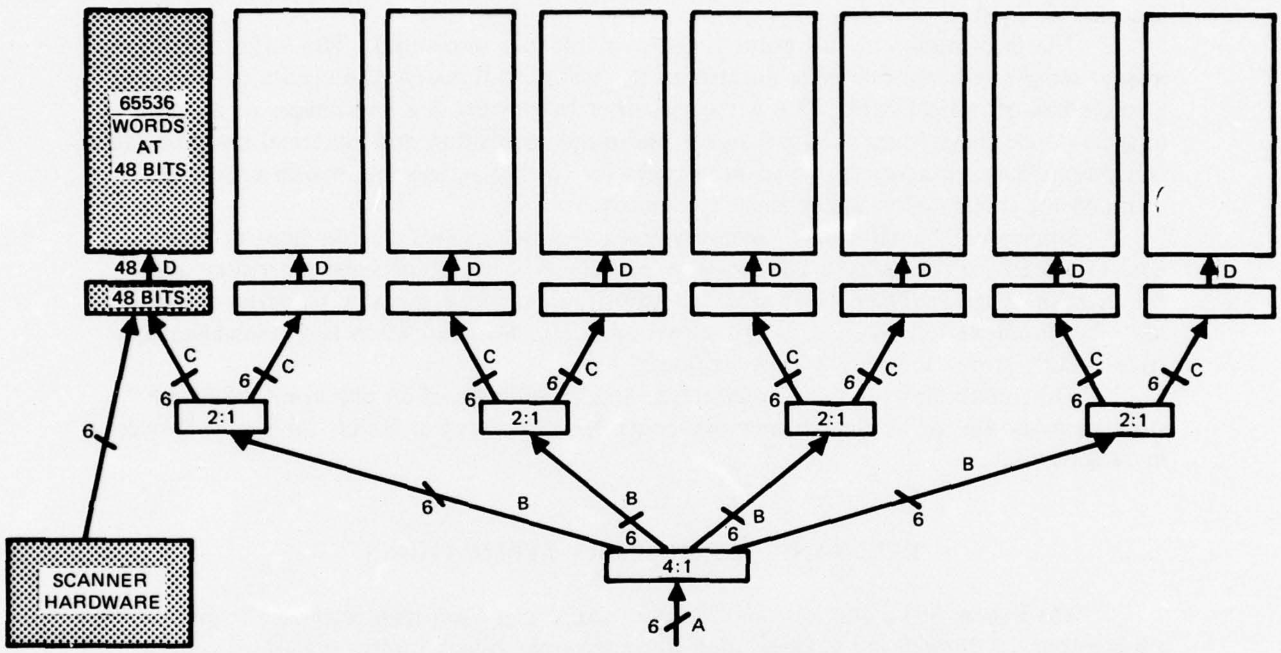
RELEVANCE TO MILITARY APPLICATIONS

The Frame Store Memory and Memory Controller have high relevance to military applications. Although the present application is image video storage, manipulation, and retrieval, the high speed and wide work width can be applied to voice and sonar frequency spectrum analysis, correlation, and event recording of digitized sampled data at a bandwidth up to 5 megahertz.

MEMORY CHARACTERISTICS

Postal Service goals require the acquisition of image data at the aforementioned rate of 84 megasamples per second. Previous investigations at NELC have led to the conclusion that 2^6, or 64, levels of data are adequate for the acquisition and display of continuous tone images. The product of the 84 megasamples per second times the 6 bits per sample defines the input data rate for the frame store memory at 504 megabits per second.

Although not a conclusive fact for this program, previous work at NELC has indicated that a resolution of 200 by 200 picture elements (pels) in the original picture image is adequate for continuous tone photographs. This yields a requirement for a storage capacity of 40 000 pels per square inch. When multiplied by the 6 digits per pel, the memory capacity becomes 240 000 bits per square inch. From these calculations it can be seen that a total capacity of 22.44 megabits will be required to store the total image data for an 8½-by-11-inch page of copy.



REQUIRED DATA RATES			
SYSTEM LINE	MEGAPELS PER SECOND	BITS WIDTH	MEGABITS PER SECOND
A	84	6	504
B	21	6	126
C	10.5	6	63
D	1.3125	48	63

Figure B1. Full frame memory.

In this manner the acquisition rate and total capacity for a frame store memory for Postal Service applications have been defined. The next task is to equate these requirements to the availability of reliable, low-cost, off-the-shelf memory systems which will satisfactorily perform in this application. It is highly desirable, if not mandatory for the developmental system, that the memory have random access memory (RAM) capability. Future production equipments may utilize less expensive serial memories; however, they are not suitable for experimental investigations. Low-cost memories meeting this RAM requirement are metal oxide silicon (MOS) dynamic devices. At the time of purchase, dynamic MOS RAMs had a read or write cycle time of 0.5 – 1 microsecond (plus about 2% for refresh).

Since these memory rates are slower than the digitized video acquisition rate, some tradeoffs in the architecture of the frame store memory are required. In order to accommodate the acquired incoming image and the required output refresh rate (when the memory is used to display the acquired images), the memory system processes wider words at lower rates. An explanation of how the parameters are related is given in the next section.

The considerations in the tradeoff analysis include Postal Service goals; available, low-risk hardware; and cost constraints. The tradeoff defines a memory system having the basic characteristics shown in table B1.

TABLE B1. Frame Store Memory Characteristics.

Number of bits	3 145 728
Word width	48 bits
Read access time	450 ns
Read/write cycle time	650 ns

ARCHITECTURAL TRADEOFFS

The storage required for a complete page of information, meeting the Postal Service speed and resolution requirements, is a total of 3.74 million video samples of 6 bits each at the rate of 84 million video samples per second. In its simplest form this would amount to a 3.74-megaword by 6 bit memory having a write cycle time of less than 12 nanoseconds. A memory organized in the above fashion is not an efficient solution. However, the desired results can be achieved by utilizing a different memory architecture and a scheme of demultiplexing. When the video information is arriving at 11.9 nanoseconds per sample, it can be considered to be a multiplexed data stream. A demultiplexing operation would separate the data into a wider but slower data path. Demultiplexing is accomplished by saving η consecutive video samples ($\eta > 1$) in a register of length equal to 6η bits (6 bits per pel). The resulting data words can then be handled by subsequent logic at $\frac{84}{\eta}$ megawords per second. For example, if η=2, then the 84 megapel per second video data would be converted to 42 megaword per second data with each word containing 2 pels, or 12 bits. The eventual choice of a value for η is determined by the video rate and the available MOS RAM cycle times. There are still other factors affecting the eventual memory architecture. These are the individual memory devices used to implement the memory system, refresh requirements, and the required support hardware.

At the time the memory system was procured, the state-of-the-art memory device was an MOS dynamic RAM organized as 4k words by 1 bit. The operating speed of the typical 4k memory chip was in the 600–900-nanosecond region, with faster chips available at premium cost. An additional factor to be considered in selection of a memory system architecture is the fact that industry has prepackaged and offers on an off-the-shelf basis memory systems organized in multiples of 8-bit words. By examining table B2, it can be seen how an increase in the multiplex ratio to 64 produces a memory system 384 bits wide and achieves the required speed reduction with available devices. The complete memory system would therefore be 65k words by 384 bits with acceptable read/write cycle times of approximately 750 nanoseconds. This memory would be packaged in approximately 9-1/2 cubic feet, including the power supplies. The current cost of such a memory system at approximately 0.5 per bit is in the $100–125k category.

TABLE B2. EFFECTS OF MULTIPLEX RATIO η

Multiplex Multiplex Ratio	Word Width, bits	Memory Frequence, MHz	Word Clock Period, ns
1	6	84	11.9
2	12	42	23.8
4	24	21	47.6
8	48	10.5	95.2
16	96	5.25	190.5
32	192	2.62	381
64	384	1.31	762

THE NELC MEMORY SYSTEM

The memory system procured for scanner testing and developmental work at NELC need not be large enough to contain an entire video page. Therefore, a subset of the entire frame store memory was selected with a multiplexed ratio η equal to 8 which yields a 65k-word by 48-bit memory. This memory system therefore is a one-eighth slice of the entire frame store memory and can store a maximum of one-eighth of a page at the required resolution. Figure B1 shows how this memory segment can be combined with seven other similar units to perform the full page storage. Line A in the figure is the input 84 megapel per second video input. It is 4:1 demultiplexed to line B, which represents four 21 megapel per second lines. Four parallel 2:1 demultiplexers reduce the data to those shown in line C, or 8 each 10.5 megapel per second line. The 10.5 megapel data stream in line C is then demultiplexed further by a factor of 8 to line D, which is the 1.3 megaword per second rate compatible with the memory system. The portion of the entire system that exists at NELC is the shaded area with an input at line C from the image scanner test bed operating at a maximum of 10.5 megapels per second.

MEMORY SUPPORT AND CONTROL HARDWARE

The memory control and support hardware constructed at NELC performs three principal functions: input digital video from scanning hardware to the frame store memory, display the stored image on a cathode ray tube (raster type display), and process or analyze the digital video image data as appropriate. The memory controller has been constructed from off-the-shelf, state-of-the-art, TTL digital hardware and based on the Intel 3000 series LSI computing devices.

The hardware is composed of seven major functional blocks as shown in figure B2. In operation the input video from the scanning hardware is packed or demultiplexed from 6 to 48 bits. The 48-bit words, each containing eight 6-bit video samples, are transferred to the memory via a data bus and the memory I/O logic. The same memory I/O interface logic is used to extract the video data from memory and present them to the output logic. The output logic contains the output multiplexer, which takes 48-bit words and serializes the eight 6-bit video samples into the same digital video sequence originally received. The output logic also contains hardware with the ability to select any bit precision between one and six, or any bit plane between one and six, while maintaining the full dynamic range of the D/A converter and display. The system contains a manual control panel which can display the contents of any memory word or input a 48-bit word to any memory location. In addition, any one of 10 internal scratch pad registers may be displayed or modified from the control panel. Other manual mode and control functions are also provided. A set of peripheral input/output ports permits communications between the memory, the control system, the image analyzer system, a magnetic tape unit, a CRT display terminal, and any other appropriate peripheral device not now included. The upper left hand block in figure B2 (the processing array) is composed of 24 each Intel 3002 central processing elements.

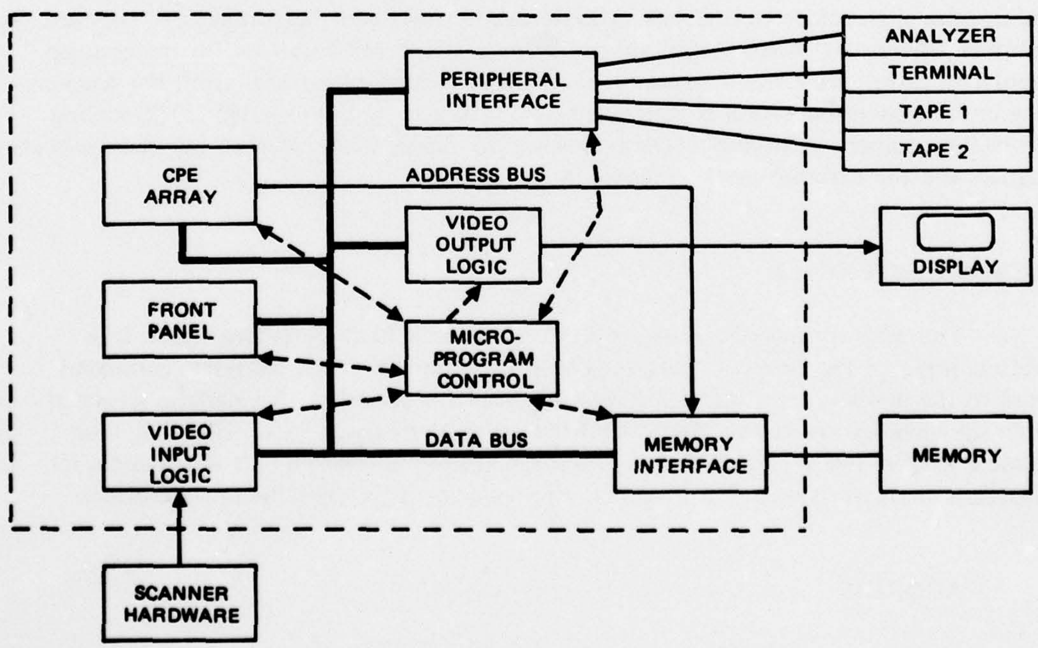


Figure B2. Simple block diagram.

These devices are used to generate and maintain memory address for capture and display as well as process data for interface to the peripheral I/O devices. They automatically, therefore, provide the ability to process video data from the memory. Overall system control is maintained by the microprogram control unit (one Intel 3001) and its associated micromemories. All bit-level control functions performed in the system are derived from this control area. Extensive versatility is provided in the microprogram control structure to enable both macro and micro level (software or firmware) control of the entire system. A detailed description of the operation of each individual subunit within the memory control system follows.

MEMORY CONTROLLER THEORY OF OPERATION

SCANNER INPUT AND PACKING LOGIC

The scanner input interface performs two functions. First, the appropriate differential line driver/receiver circuits are provided for direct electrical interface to the scanner equipment. In figure B3, the 6 data inputs, representing the binary coded equivalent of the sampled video, are presented as an input to 8 independent 6-bit registers. As each new video sample arrives, it is loaded into a new 6-bit register under control of a 3-bit binary counter and 3-to-8 decoder, all driven by the external scanner clock. When all eight 6-bit registers have been loaded, the next clock pulse simultaneously loads all 48 bits into the second register and relaods the first 6-bit register. In this manner a continuous 6-to-48-bit demultiplex operation is performed and the resulting 48-bit words are enabled onto the Secondary Data Bus (SDB) for entry into the rest of the system. Two other control signals received by the scanner input interface are "Data Available," which is a frame gate, and the "Line Sync" signals. These signals are used by the microcontrol structure to maintain synchronization between the scanner and the memory address generation. Also, the microcode sends a "Capture" command to the scanner hardware to initiate a frame capture. During the capture of a frame from the scanner, the entire system operation is controlled by and timed by the external clock coming from the scanner. A timing diagram showing the relationship between the various control signals and the external clock is shown in figure B4.

MEMORY INTERFACE

The memory interface logic is divided into four basic parts (see figure B5): address input to the memory, data transmission to and from the memory, command lines to the memory, and status information from the memory. All signals associated with the memory are transmitted over differential twisted-pair lines. High common mode rejection and a 15-volt common mode range of the twisted-pair line drivers, receivers, and transceivers (75114/115/117) provide for highly reliable data transfers.

ADDRESS

The address information is generated in the central processing arrays and presented to line drivers via the Memory Address Register Bus (MARB). The address

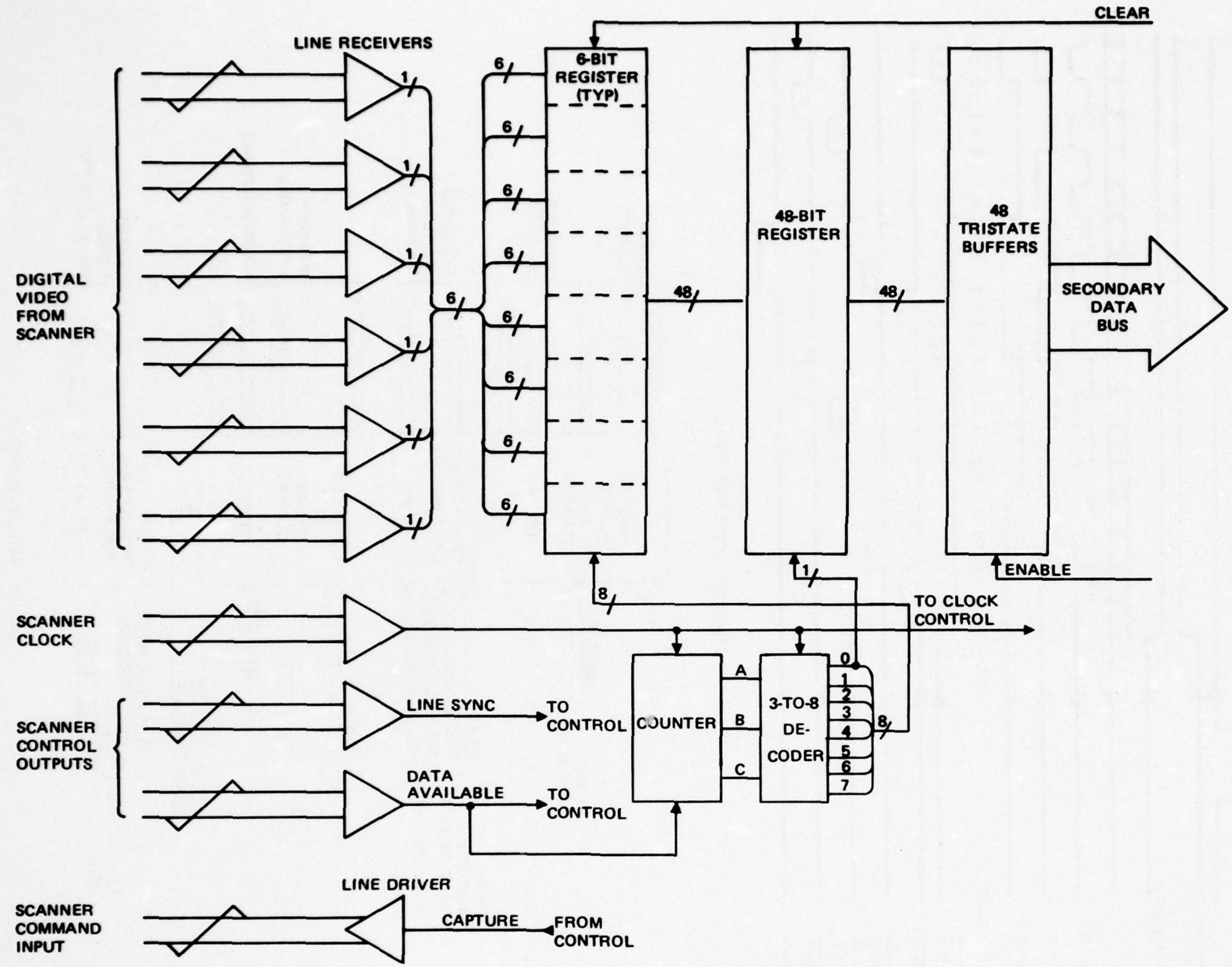


Figure B3. Scanner input & packing logic.

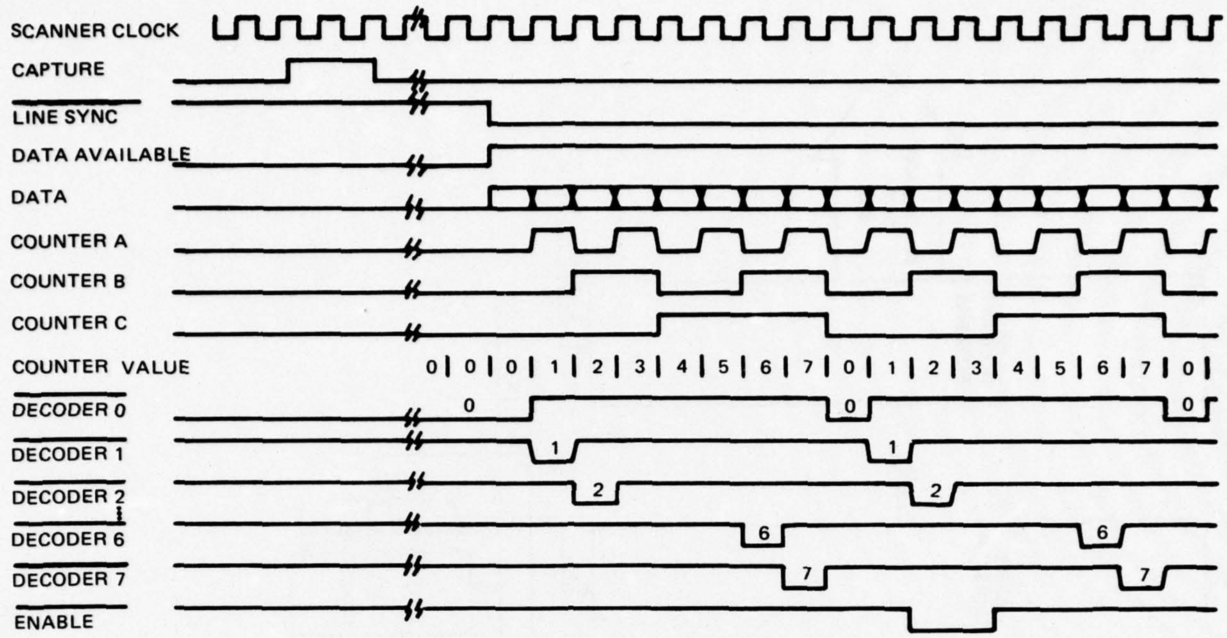


Figure B4. Input logic timing

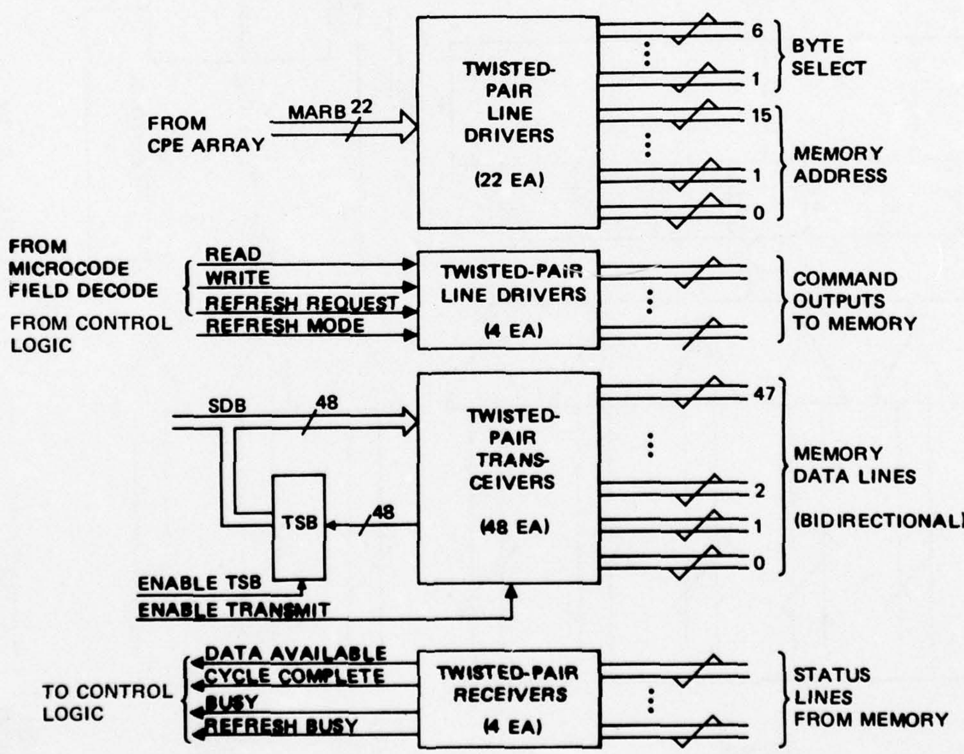


Figure B5. Memory Interface.

information is actually divided into two parts. One is a 16-bit address field selecting any one of the available 65k memory words. This address specifies either the read or the write location in memory. In addition six independent byte select lines are provided which may selectively enable or disable the write operation on any or all of the selected 8-bit bytes. The byte select inputs are not active for read operations.

DATA LINES

The 48 data bits are transmitted to and from the memory over a common 48-pair cable. Forty-eight twisted-pair transceivers operate much as do the twisted-pair driver/receivers used for the memory address and command lines. The only difference in the memory data lines is that they operate in half-duplex mode; that is, data transmission occurs in both directions (to or from the memory) over the same lines but not at the same time. The data source and destination in the control system is a single 48-bit data bus called the Secondary Data Bus (SDB).

COMMANDS TO MEMORY

There are five control signal input lines associated with memory. These are the read, read enable, write, and refresh request commands and the refresh mode control line. The memory system will respond to input commands with one of four status or control replies – data available, cycle complete, busy, and refresh busy. These commands and status lines are used in various ways to accomplish one of the three possible memory functions (read, write, or refresh).

READ OPERATION

The read operation is performed by simply transmitting the appropriate memory address to the memory and initiating a read command pulse. The memory system will respond with a busy signal while the memory itself performs the function and waits for required propagation delays. After the minimum access delay, the data from memory will be available on the 48-bit data lines. The memory will then respond with a data available pulse, at which time the memory interface tristate buffers may be enabled onto the SDB. The time delay or propagation delay from initiation of the read command until the memory responds with the data and the data available pulse is approximately 450 nanoseconds. The memory system, however, is not yet ready to accept another command. The busy line will remain true for another 200 nanoseconds while internal propagation delays in the memory system settle. When the busy signal is removed, the cycle complete pulse will be sent by the memory indicating that the present cycle has been completed. It is convenient that the memory system contains its own 48-bit data register. This permits the memory controller to return at a later time (provided a subsequent read or write operation has not been performed) and simply reenable the memory tristate buffer to reread the same data word. It is not necessary to generate another address and read command.

WRITE OPERATION

In the write operation the address must be presented to the memory as in the read operation. The write operation is initiated by a write pulse, again similar to the read operation. The one important difference between the write operation and the previous read operation is the fact that the six byte select lines must be appropriately controlled. A true on a byte select line will permit the write operation to occur in the memory in the selected 8-bit byte. Any or all of the six 8-bit bytes may be enabled in this fashion independently. The response of the memory system to a write operation is identical to that of a read operation.

REFRESH

Since the memory system is constructed from dynamic MOS memory chips, the data within the memory are volatile and must be refreshed on a periodic basis. According to the worst-case specifications, the entire memory system must be refreshed every millisecond. This requires that 64 refresh request signals be sent to the memory every millisecond. The specification for full refresh every millisecond is determined by the worst-case conditions, particularly at elevated temperatures. In a controlled temperature environment this specification may be relaxed considerably.

The memory system may be refreshed in two different ways. If desired, the refresh requirement can be met by the memory system itself with its own internal logic. With the refresh mode signal in the appropriate state the memory system will generate refresh requests on a periodic (but asynchronous) basis and satisfy the minimum refresh requirements. The memory system during automatic refresh will automatically disallow any read or write commands attempted during the refresh cycle. A busy signal called refresh busy is transmitted by the memory system during refresh operations to inform the control hardware that the memory is not available due to refreshing. The timing of the refresh cycle is approximately the same as that of a read or write cycle.

During certain types of operation with the memory (namely, capture and display of video data) it is not permissible to allow interruption of the read or write cycle by automatic refresh. During such times the refresh mode control is switched to inhibit automatic refresh. The refresh requirement must then be met by the control unit using the refresh request signal. The refresh request signal initiates a refresh cycle exactly as does the internal automatic refresh. It may, however, be controlled in time, or synchronized to other operations of the system. In actual application this refresh request signal is sent to the memory during video line sync times where it will not interfere with the storing or displaying of video data.

Figure B6 details the relative timing between the memory command, address, data, and status reply.

VIDEO UNPACKING AND OUTPUT LOGIC

In order to display the captured image, the frame store memory and controller are used as a refresh memory and sync generator for a raster-type display monitor. Forty-eight-bit memory words, containing eight 6-bit video samples, represent eight pels of a

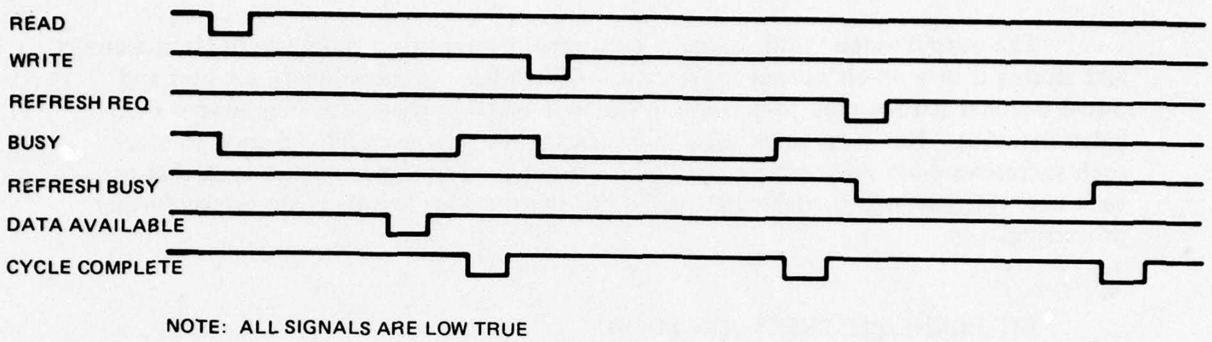


Figure B6. Memory timing.

video line. Address generation for the memory read cycles is performed by the CPE arrays. Since the captured image was stored on a sequential line-by-line basis, and the TV display monitor generates an interlaced raster, some address calculations must be performed at the conclusion of each video line to achieve interlace. In addition to display video refreshing the CRT, the control section of the system generates independent horizontal and vertical sync pulses for the monitor timed to achieve a 2-to-1 interlace. Standard 525 or other standard line sync rates are not required, since the Conrac RQA/B monitor will phase lock and maintain synchronization over a wide range of input horizontal and vertical frequencies. The system has the ability to modify these rates on the fly during vertical retrace time to alter the display parameters. Additional functions performed by the video output logic include the remultiplexing of eight 6-bit video samples into a sequence of 6-bit video pels having a frequency eight times faster than that of the 48-bit memory words. Subsequent logic is included to select any bit precision between one and six bits or any bit plane between one and six for presentation to the D/A converter and the monitor. There is no loss in analog dynamic range during either of these conversions.

A GFE 9-bit-plus-sign D/A converter capable of operating in excess of 100 MHz is used to generate the analog video for the display. Although this converter represents a considerable overkill in speed for the system, it was available to the program at no cost. A variety of commercial 6-or-more-bit D/A converters is available to perform

this function. Simple operational amplifier level shifters are provided to convert the digital sync signals to those which are recognizable by the monitor. Figure B7 is a block diagram of the video output and unpacking logic and the analog interface to the display.

VIDEO OUTPUT MULTIPLEXER

The output video multiplexing is performed by reading a 48-bit word from memory and storing it in a 48-bit output register via the data bus. A 3-bit binary counter and 3-to-8 decoder is then used to selectively enable 6-bit-wide tristate buffers onto a 6-bit video data bus. The same clock used to increment the binary counter is used to clock each successive 6-bit video sample to a 6-bit retiming register in a manner such that as each new video sample is enabled onto the bus the previous sample is stored for further processing.

BIT PLANE/BIT PRECISION LOGIC

The bit plane/bit precision logic must select either one of the six bit planes, or any one of the six possible bit precisions, to be transmitted to the D/A converter. It is important that no loss of analog dynamic range occur during the process. This is accomplished by either selecting the desired bit plane or (exclusive or) selecting a desired bit precision. The 6-bit-wide digital video is presented simultaneously to an 8-to-1 multiplexer for bit plane select and to the second stage of logic which may or may not be used to select the desired bit precision. The logic circuitry implementing this function operates in the following fashion (see fig B7). The bit plane selector is a simple 8-to-1 multiplexer while the bit precision selector is a hex 2-to-1 multiplexer set with additional copy logic used to maintain full analog dynamic range. In operation, the decision sequence involves first selecting a bit plane between one and six or no bit plane. If a particular bit plane is selected, the bit precision 2-to-1 multiplexers are switched to the bit plane multiplexer output. The bit plane control lines select one of the six bit planes and connect it to the A inputs of all six bit precision multiplexers. If bit plane 0, which is nonexistent, is selected, then the 6-bit digital video is selected and the B input to the bit precision multiplexers is enabled.

Copying logic (not detailed in fig B7 for simplicity) in the bit precision selectors is what maintains the full analog dynamic range in the D/A output. Consider a bit precision selection of five as an example. The high-order five video bits are connected through line driver/receiver circuits to the high-order five bits of the D/A converter. The low-order bit of the D/A converter is connected to the most significant video bit, thereby duplicating the most significant bit in the least significant bit position. This connection assures that a video sample of value 00_8 will be transmitted to the D/A converter as a full 6-bit-wide 0 word and the maximum value, 77_8, will also be connected to the D/A converter as a 77_8. Subsequent lower bit precision selections are implemented in a similar fashion in which the highest selected video bits are connected straight through and the unused low-order positions are copies of the high-order positions. Any connection other than this scheme either sacrifices D/A dynamic range or produces non linear steps in the video output.

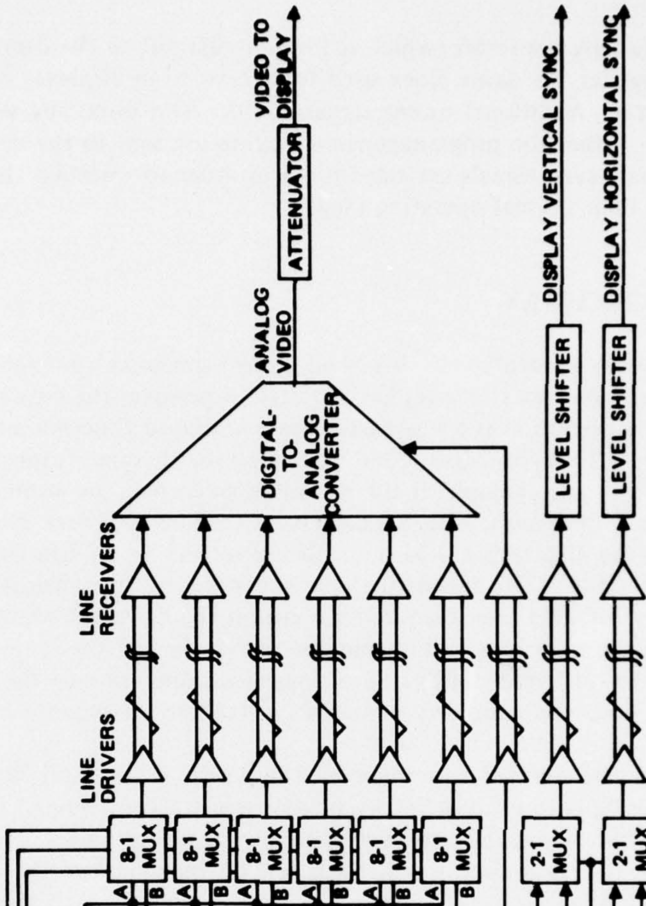


Figure B7. Video output & unpacking logic.

Since the D/A converter (which is located adjacent to the display) contains its own retiming register, the same clock used for the video multiplexer is transmitted to the D/A converter. Additional timing signals are the horizontal and vertical sync pulses for the display. Either the program-generated syncs are sent to the display, or in their absence, automatic sync signals are substituted in order to maintain the monitor phase locked loops in their normal operating range.

PROCESSING CIRCUITRY

The memory controller (as described above) generates command functions for the memory and monitors status replies in order to perform the required data transfers. Since the capture operation is a line-by-line, noninterlaced function and the display monitor requires a TV type 2-to-1 interlaced video input, some form of address calculations is required. For example, if the incoming video data are stored sequentially during the capture operation, then for display of that image, every other video line must be presented to the display for field one and the second set of alternating lines must be displayed on field two. This means that the controller must sequentially output the video on line one of field one, then add a constant (equal to the number of words/line) in order to skip the next line, and output the second line of the same field. In addition to address calculation, direct arithmetic or logical manipulation of the video image is necessary. The processing circuitry comprises a standard Arithmetic Logic Register Unit (ALRU).

The hardware selected to implement the ALRU is the Intel 3002 Central Processing Element. The 3002 chip is an Schottky bipolar large-scale-integrated circuit containing a 2-bit slice of a complete ALRU. It is expandable by use of additional chips, and optionally lookahead carry, to any desired word width in 2-bit increments. The unit contains an arithmetic logic unit recognizing 39 simple microcommands. A total of 13 registers is provided including an accumulator and memory address register (with outputs accessible) and 11 scratch pad registers.

The complete memory controller utilizes 24 of the 3002 chips to assemble a complete 48-bit processing section plus three additional (Intel 3003) fast lookahead carry chips. The 48-bit-wide ALRU provides all the flexibility necessary for address generation, memory control, and video processing that is now required or might be required in the future. A detailed description of the operation of the 3002 devices is available from Intel corporation publications. The Intel series 3000 reference manual (98-221A) contains data sheets covering the 3002 central processing element and all the other 3000 series compatible devices. Figure B8 shows the 3002 block diagram and summarizes the microfunctions it implements.

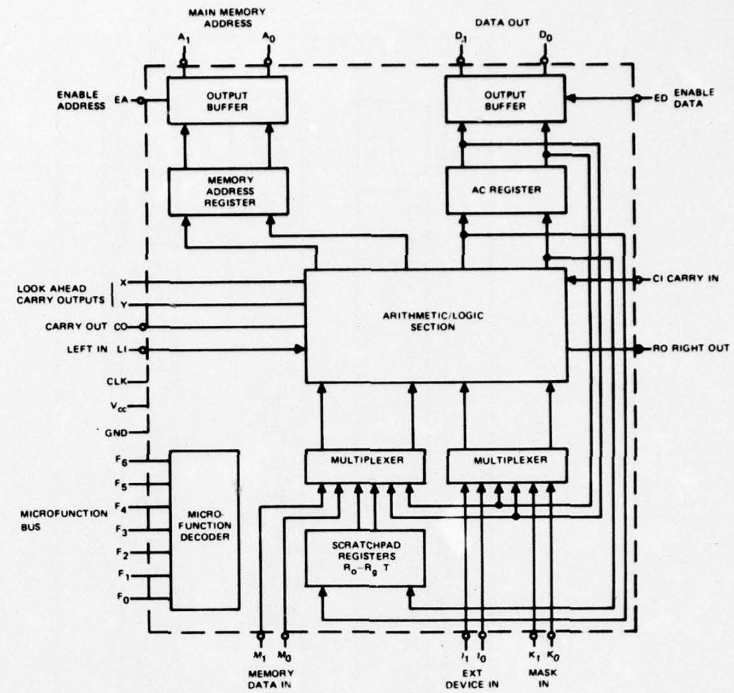
MANUAL CONTROL PANEL

In order to operate the system, a manual data display and function control panel is provided. It is possible, from the control panel, to load 48-bit words into the accumulator or any R register, display the contents of the accumulator or any R register, and control the clock and mode functions. Figure B9 shows the layout of the various switches and displays available.

F-GROUP	R-GROUP	MICROFUNCTION	
0	I	$R_n + (AC \wedge K) + CI \rightarrow R_n, AC$	
	II	$M + (AC \wedge K) + CI \rightarrow AT$	
	III	$AT_L \wedge (\overline{I_L \wedge K_L}) \rightarrow RO$	$LI \vee [I_H \wedge K_H) \wedge AT_H] \rightarrow AT_H$
		$[AT_L \wedge (I_L \wedge K_L)]$	$[AT_H \vee (I_H \wedge K_H)] \rightarrow AT_L$
1	I	$K \vee R_n \rightarrow MAR.$	$R_n + K + CI, \rightarrow R_n$
	II	$K \vee M \rightarrow MAR$	$M + K + CI \rightarrow AT$
	III	$(\overline{AT} \vee K) + (AT \wedge K) + CI \rightarrow AT$	
2	I	$(AC \wedge K) -1 + CI \rightarrow R_n$	(SEE NOTE 1)
	II	$(AC \wedge K) -1 + CI \rightarrow AT$	
	III	$(I \wedge K) -1 + CI \rightarrow AT$	
3	I	$R_n + (AC \wedge K) + CI \rightarrow R_n$	
	II	$M + (AC \wedge K) + CI \rightarrow AT$	
	III	$AT + (I \wedge K) + CI \rightarrow AT$	
4	I	$CI \vee (R_n \wedge AC \wedge K) \rightarrow CO$	$R_n \wedge (AC \wedge K) \rightarrow R_n$
	II	$CI \vee (M \wedge AC \wedge K) \rightarrow CO$	$M \wedge (AC \wedge K) \rightarrow AT$
	III	$CI \vee (AT \wedge I \wedge K) \rightarrow CO$	$AT \wedge (I \wedge K) \rightarrow AT$
5	I	$CI \vee (R_n \wedge K) \rightarrow CO$	$K \wedge R_n \rightarrow R_n$
	II	$CI \vee (M \quad K) \rightarrow CO$	$K \wedge M \rightarrow AT$
	III	$CI \vee (AT \wedge K) \rightarrow CO$	$K \wedge AT \rightarrow AT$
6	I	$CI \vee (AC \wedge K) \rightarrow CO$	$R_n \vee (AC \wedge K) \rightarrow R_n$
	II	$CI \vee (AC \wedge K) \rightarrow CO$	$M \vee (AC \wedge K) \rightarrow AT$
	III	$CI \vee (I \vee K) \rightarrow CO$	$AT \vee (I \wedge K) \rightarrow AT$
7	I	$CI \vee (R_n \wedge AC \wedge K) \rightarrow CO$	$R_n \bar{\oplus} (AC \wedge K) \rightarrow R_n$
	II	$CI \vee (M \wedge AC \wedge K) \rightarrow CO$	$M \bar{\oplus} (AC \wedge K) \rightarrow AT$
	III	$CI \vee (AT \wedge I \wedge K) \rightarrow CO$	$AT \bar{\oplus} (I \wedge K) \rightarrow AT$

NOTES:

1. 2's complement arithmetic adds 111 . . . 11 to perform subtraction of 000 . . . 01.
2. R_n includes T and AC as source and destination registers in R-group 1 microfunctions.
3. Standard arithmetic carry output values are generated in F-group 0, 1, 2 and 3 instructions.



FUNCTION GROUP	MICROFUNCTION INPUT F_6	5	4
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

REGISTER GROUP	REGISTER	MICROFUNCTION INPUT F_3	2	1	0
I	R_0	0	0	0	0
	R_1	0	0	0	1
	R_2	0	0	1	0
	R_3	0	0	1	1
	R_4	0	1	0	0
	R_5	0	1	0	1
	R_6	0	1	1	0
	R_7	0	1	1	1
	R_8	1	0	0	0
	R_9	1	0	0	1
	T	1	1	0	0
	AC	1	1	0	1
II	T	1	0	1	0
	AC	1	0	1	1
III	T	1	1	1	0
	AC	1	1	1	1

Figure B8. 3002 block diagram and instructions

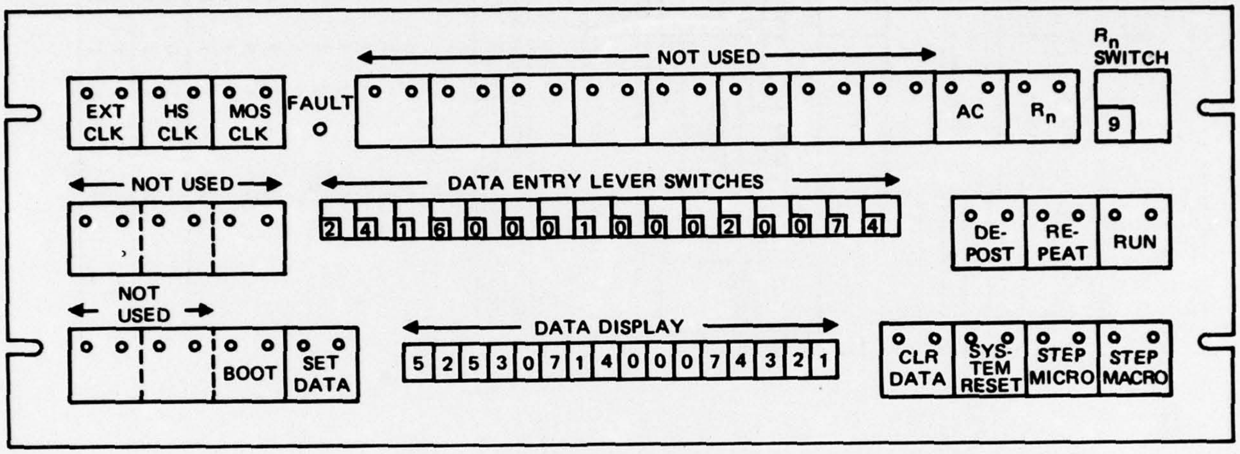


Figure B9. Manual control panel.

DATA IN/DISPLAY

Sixteen octal coded lever switches are provided to enter 48-bit data words into the system. Solid-state buttons and an additional decade lever switch permit data entry to any R register or the accumulator. These registers may be examined on 16 octal coded displays located directly below the lever switches. Operation of the manual data transfers is as follows.

A register is selected by touching the accumulator button or the R_n button with R_0 - R_9 selected on the R_n switch. Each time the accumulator or R_n button is touched, the display presents the contents of the selected register. Data entry is accomplished by setting the desired register, and touching the set button. The data on the lever switches will be transferred to the selected register and the contents of that register will be displayed. A clear button is also provided. Operation is like that of the set button except that the lever switches are ignored and all zeros are loaded into the selected register and displayed.

A deposit button is provided to enable the manual entry of 48-bit words into any selected main memory location. This is accomplished by the following procedure: first, register R_7 is selected and the desired memory location is set into the low-order 16 bits. The desired data word to be loaded into memory is then set on the lever switches and the deposit button is touched. This operation inputs data from the lever switches to the memory location specified by R_7 and subsequently displays the contents of the memory location ($R_7 + 1$). Further details on the examine and deposit functions are included in the microprogramming section.

CLOCK CONTROL

Three switches are provided in the upper left corner of the front panel which permit manual selection of the system clock source. During capture of video data from the scanning hardware the external clock position must be selected. In this mode of operation the entire system is clocked and timed by use of the clock transmitted from the scanning hardware. This synchronizes the two systems and avoids further retiming hardware. The other two clock source buttons select internal clocks of two speeds. The HS (high speed) clock is the clock used for display of video data or execution of other programs at video rates. The MOS clock is a counted-down version of the HS clock and is used for lower-speed functions. Clock source selection may also be performed under program control. Further details are included in the microprogramming section.

MODE CONTROL

In the lower right hand portion of the control panel the mode control buttons are located. These switches are used to command the system to execute commands in various ways. Instructions can be run, stepped, or repeated by use of the mode control buttons, and a master system reset button is also included. A complete description of the operation of these controls must, however, be delayed until after the sections on macro and micro programming.

FAULT LIGHT

There are certain error conditions detectable by the microprogram in the machine where a convenient fault point is available. If these conditions occur, the machine suspends all operation and turns on a fault light. The contents of registers and memory locations may be examined and the system may resume operation after a system reset.

BOOTSTRAP

The last special function of the control panel is provided by the bootstrap button. This button is only used to initialize the system. Its function is to initiate a special microprogram which loads the main memory with all constants and monitor instructions

necessary for further operation using the terminal. The data source necessary to implement this automatic load function is a magnetic tape unit and therefore no manual setup operations are required. The power-up procedure is simple: load the appropriate magnetic tape, apply power to the system, and touch the bootstrap button. All system operation may then be performed from the Tektronix CRT terminal.

PERIPHERAL INTERFACE

In order for the memory and control system to communicate command and data information to peripheral devices, interface hardware is provided. There are three groups of interface hardware (not including the scanning hardware or the memory), each with multichannel capability. The peripheral devices currently connected to the interface hardware are the tektronix 4023 CRT display terminal, the image analyzer hardware, and magnetic tape equipment.

IMAGE ANALYZER INTERFACE

The image analyzer, constructed to generate image statistics at video rates, is connected to the memory controller via an 8-bit parallel data channel. The interface allows the memory controller to send commands to the analyzer hardware for control purposes. It is also possible to transmit digital video to the analyzer, from either main memory or magnetic tape, for image statistics generation. Subsequently, the result of the selected analysis can be transferred back to the memory controller for further processing or data reduction. Besides the 8-bit data field, the interface includes a 2-bit function control field and a 2-bit address field. It is therefore possible to connect three additional hardware peripheral devices to this interface channel by using the 2-bit address field as a device select field.

TERMINAL INTERFACE

The GFE Tektronix 4023 CRT display terminal is included in the system for control purposes as well as display of program and statistical information. The interface to the terminal is similar to the image analyzer hardware in that data are transferred as 8-bit characters. The characters are transferred bit serial, however, by use of a 9600-baud RS-232C interface. The memory controller includes the serial-to-parallel, parallel-to-serial, and timing logic required for the bit serial interface. Subsequently to the parallel/serial/parallel conversions and retiming necessary, the interface operates in an 8-bit parallel fashion. It is therefore possible to use the terminal to display decimal image statistics and alphanumeric information in a columnar format. A compatible Tektronix hard-copy unit is also available to facilitate the generation of hard-copy permanent records. The terminal interface, like the analyzer interface, also includes a 2-bit device select field. This permits the interface to communicate with three additional RS-232C type devices.

MAGNETIC TAPE INTERFACE

Since the main memory in the system is dynamic MOS volatile memory, all information contained in the memory is lost during power failure or normal power shutdown. Since large amounts of command and program information may be contained in the memory, it is necessary to provide some form of nonvolatile magnetic storage. This storage can in addition be used to store complete video frames of information at the required Postal Service resolution. Images so stored can be retrieved at subsequent times, reprocessed, or otherwise manipulated without the necessity of a new capture.

Since the magnetic tape data transfers require a control register wider than the 8 bits of the other interfaces, and require block transfers of data, the interfaces are considerably different from those described above. Two magnetic tape interface channels are provided, each channel having the capability of communicating with four tape drivers. Special microroutines are provided for each tape channel to facilitate differences between the tape units available, and to facilitate the block transfers of data required. Also included are standard command register outputs and sense or status condition inputs from the magnetic tape unit to the control system.

These interface channels (relatively few in number) provide all the flexibility needed to perform the capture, storage, display, processing, and analysis of Postal Video images.

MICROPROGRAM CONTROL

A crucial part of any digital logic system is the control sequence generator. This logic block is responsible for maintaining system timing and synchronization. It generates all the necessary control signals required by the remainder of the system. This control sequencer is responsible for directing the operation of all other logic blocks within the system. Methods of implementing this control hardware fall into two general categories. Older equipment generally used a sequential state counter approach in which the entire control structure is defined by hardwired logic elements. This is perfectly adequate for smaller logic systems or for those in which changes in the control structure will not be made. Extensive hardware rework may be required in this type of control structure if minor alterations in the sequence generator output states are required. A more versatile approach in which the control structure is stored as in a bit pattern in a memory is called microprogramming. All that is required to completely alter the control structure of the machine in a microprogrammed control unit is to reprogram the micromemory. The state of all control signals required internally to the machine is stored in the micromemory either in direct or encoded form. A micromemory address generator of some type is used to select the microcontrol words one at a time.

In the NELC memory controller hardware the microprogram address generator is an Intel 3001 microprogram control unit. Two separate microprogram memories are provided for control storage. One memory is the high-speed programmable read only memory (PROM) which stores the controls required to manipulate data at video rates. This memory is supplemented by a smaller electrically alterable read only memory (EAROM) which is used at slower speeds for microprogram development, testing, and operation at low speeds.

3001 MICROPROGRAM CONTROL UNIT

The Intel 3001 microprogram control unit contains the micromemory address register and all the logic necessary to maintain proper micromemory sequencing. (Refer to the block diagram of fig 10). The microprogram address register is a 9-bit register with outputs designated MA_0 through MA_8. The content of this address register selects any one of the possible 512 micromemory locations. The register contents are synchronously determined by the next address logic one of several ways. The low-order 8 bits of the register can be loaded from the primary and secondary instruction bus inputs by taking the LD input high. After the rising edge of the clock, the data on the secondary instruction bus will be loaded into MA_4 through MA_7 and the data on the primary instruction bus will be loaded into MA_0 through MA_3. For the load operation MA_8 is always set to a logic 0. During normal microprogram execution, the next-address logic generates each successive microprogram address as a function of the current address and the address control function inputs (AC_0 through AC_6). The C and Z flag and the F latch may also affect the next microprogram address, depending on the contents of the AC_0 through AC_6 inputs. For a detailed description of this complicated operation refer to the published Intel 3001 data sheet.

Figure B11 shows how the 3001 and the microprogram address and all other microlevel system control functions. In operation, each micromemory output word contains the appropriate system controls. Also, information is fed back to the address control function input to enable the next-address logic to generate the next microprogram address. Each sequency of microinstructions causes the system to perform some desired function. The micro starting address for a particular sequence is first loaded into the microprogram address register. The sequence is then executed until completion, at which time the starting address for the next sequence is fetched. The data source for this load function may be alternately the high-order bits from a main memory word or from the front panel lever switches. By using main memory as the starting address source, a long sequence of microroutines may be generated. This provides for macrolevel control of the microprogram memory. There are currently implemented in the microprogram memory two classes of instructions. One group contains the microcode to enable the capture or display of the video data. The second group is a primitive instruction set allowing arithmetic and logic functions to be performed under macroprogram control.

SPEED CONSIDERATIONS

As described earlier, the 3001 micro control unit generates the micromemory address information for the microinstruction memory. Speed considerations have made it necessary to separate the microinstruction memory into two separate memories. Micromemory one is a low-speed UV erasable MOS EAROM. Since this micromemory can be erased and reprogrammed repeatedly, it is used for program development and testing. Its 1-microsecond cycle time requirement, however, is far too long to be useful for video routines. Micromemory two is a Schottky TTL PROM which unfortunately is not erasable. After video and other microroutines are tested and debugged in the MOS memory, they are permanently programmed into micromemory two where they operate at the video rates.

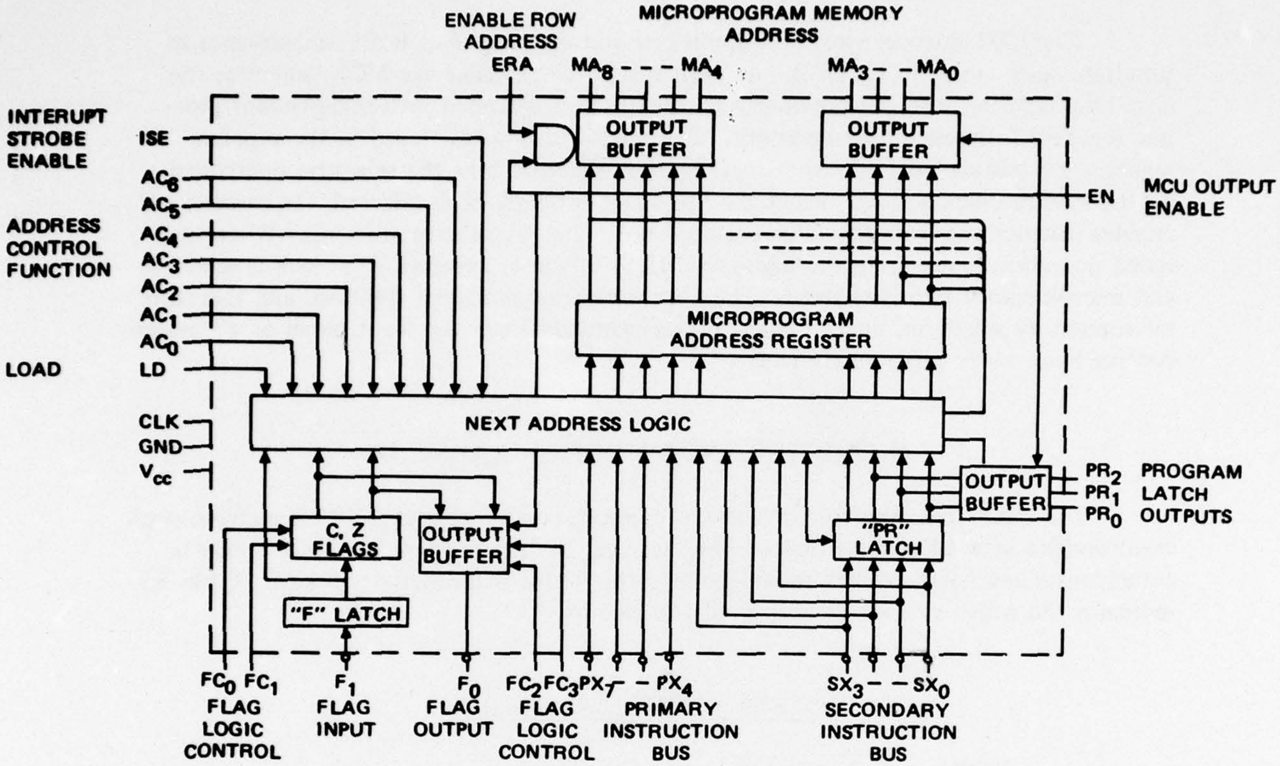


Figure B10. 3001 block diagram.

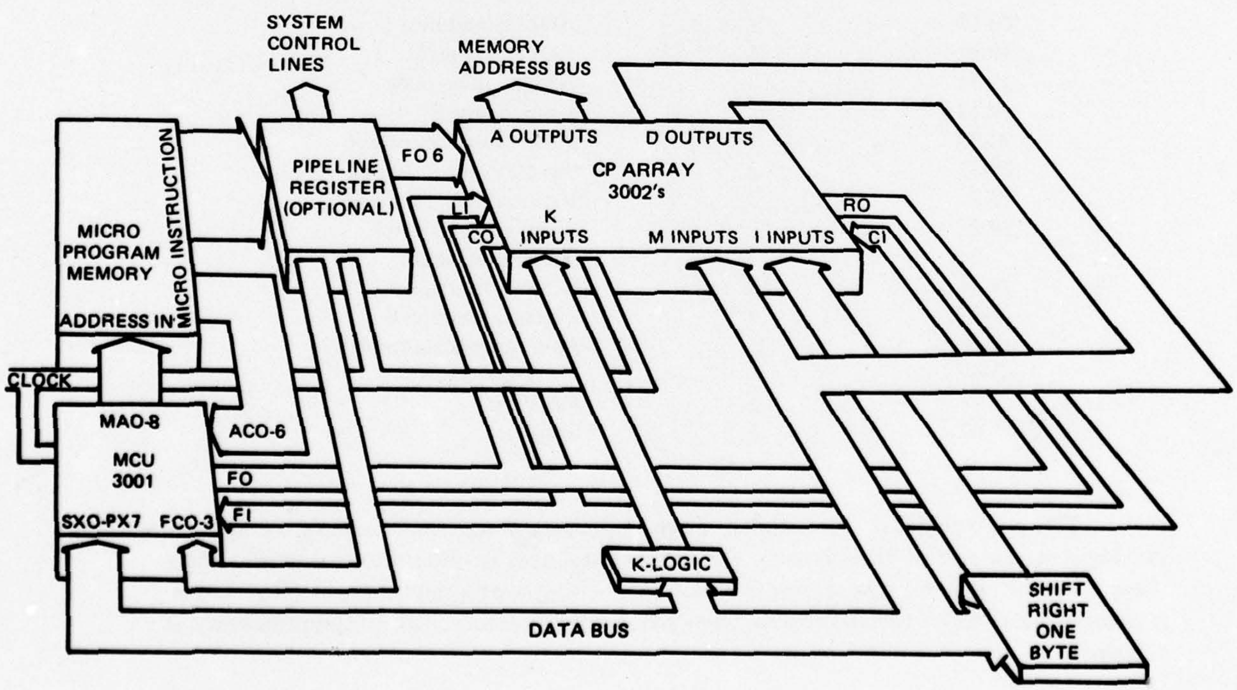


Figure B11. Microcontrol block diagram.

The 3001 microcontrol unit applies its address output to both micromemories simultaneously (refer to fig B12). At each system clock pulse the MCU generates the next microaddress, and the previous microinstruction is loaded into independent pipeline registers from each micromemory. The microinstructions stored in the pipeline registers are tristate buffered to a single microinstruction bus, the selection controlled by the system clock source. When the low-speed MOS clock is selected, the same signal enables instructions from the MOS memory onto the microinstruction bus. When high-speed operation is required, the high-speed (HS) or the external (EXT) clock is selected and micromemory two is enabled. The appropriate clock source flip-flop, and therefore micromemory selection, may be made either manually from the front panel or via system control lines under program control.

MICROCODE AND MICROPROGRAMMING

The microcode implemented in the memory controller uses a 48-bit microcontrol word divided into 14 control fields. The fact that the control word is 48 bits long is coincidental and has no direct relationship to the 48-bit main memory width. Table B3 indicates the width of each control field and its use.

TABLE B3. CONTROL WORD FIELDS

Control Word Bits	Field Width	Function
06-00	7	3001 next-address control
10-07	4	3001 flag control
17-11	7	3002 function code
19-18	2	K logic control
22-20	3	Bus data source control
25-23	3	Bus data source control
27-26	2	Main memory command
29-28	2	Clock source control
30	1	3002 clock inhibit
34-31	4	External function A
38-35	4	External function B
40-39	2	Address bus data source
45-41	5	Test input select
46	1	False test
47	1	Spare

The control fields are decoded when appropriate and the resulting signals control the logic in the rest of the system. Strings or sequences of microcontrol words implement the more general macrolevel instructions. Using a program counter (R_9) and a microroutine (Fetch) to read instructions from main memory, full programmability is achieved.

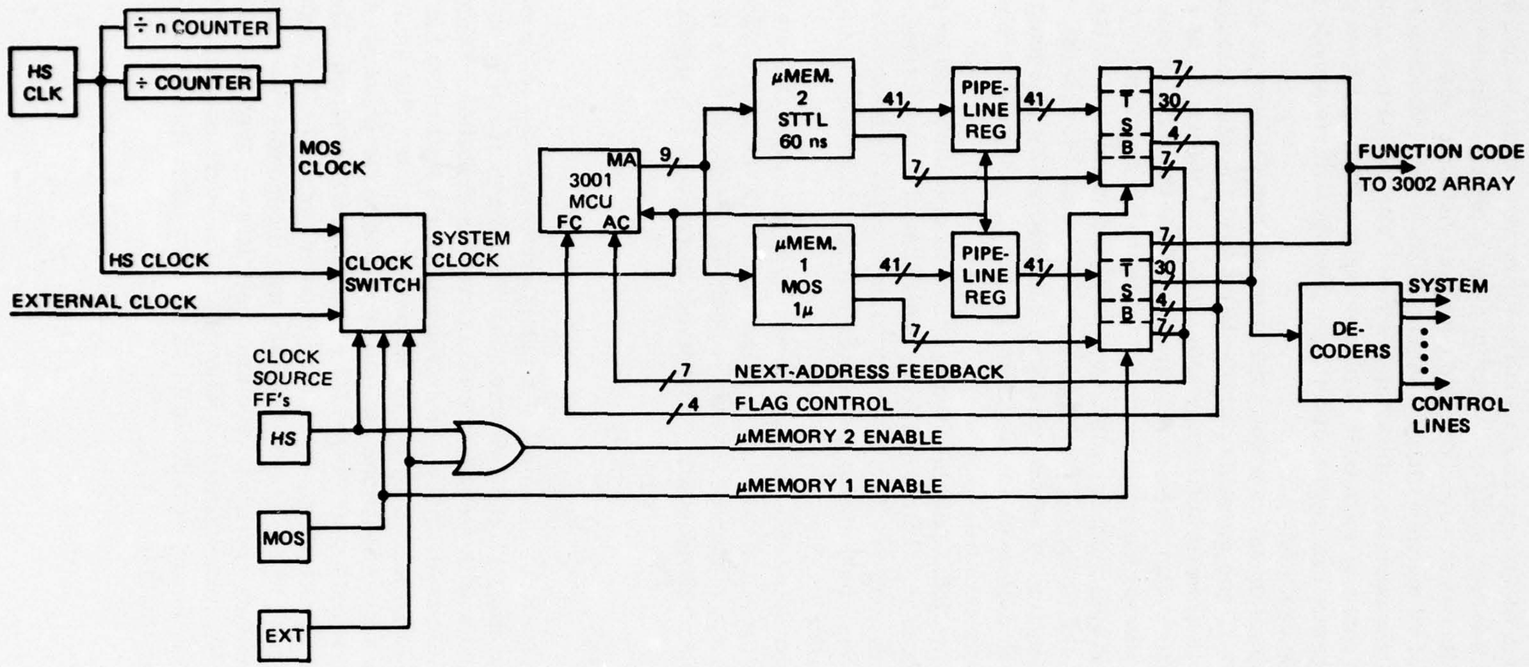


Figure B12. Microcontrol and micromemory select block diagram.

A detailed description of the microcode and the instruction set is omitted because of its extreme complexity; however, some of the information is presented in appendix A. A complete description of the microinstruction field decode is included. Also included in appendix A is a summary of all macroinstructions implemented in the microcode as well as a detailed description of the operation of each instruction. The last part of appendix A contains some sample flow charts of microcode implementing the fetch and front panel operations and the video capture and display operations. The flow charts provide a detailed map of the microcode execution.

An example of a typical operation would start at instruction $\emptyset F_H$ (upper left corner of appendix A, page BA-12 and proceed down the left side of the page through the fetch routine. This sequence of microinstructions uses scratch pad register R_9 as a program counter and fetches from main memory an instruction from the location specified by R_9. If the instruction selected happened to be an "Examine" instruction (0p Code $\emptyset 6_H$), then the microcode would jump from the lower left hand instruction to the upper right hand corner of the flow chart (appendix A) and proceed through the examine routine. The last microinstruction of all macroroutines must necessarily be a jump back to the beginning of the fetch routine located at $\emptyset F_H$. In this manner a continuous fetch/execute sequence is implemented.

An appreciation of the complexity involved in the video operations can be gained by observing the flow charts of the capture and front panel control microroutines. It should be noted, however, that with a current total of 768 microinstruction locations available in the two read only memories, only approximately one-half have been used to implement all the currently available functions.

One memory is a high-speed programmable read only memory (PROM) which stores the controls required to manipulate data at video rates. This memory is supplemented by a smaller electrically alterable read only memory (EAROM) which is used at slower speeds for microprogram development, testing, and operation at low speeds.

MODE CONTROL BUTTONS

In order to provide for manual control of program execution, four mode control buttons are provided on the front panel. Two step controls, a repeat function, and a run button provide an operator with versatile control of program execution. Testing and debugging can be done at the macrolevel or microlevel. In the instruction hierarchy, macroinstructions fetched from memory by use of the program counter (R_9) are implemented by sequences of microinstructions. In normal operation the contents of R_9 are used as an address by a microroutine (fetch) for a memory read operation. The data fetched from memory become the macroinstruction to be executed. The high-order bits of the data from memory (the OP Code) are loaded into the micromemory address sequencer at the end of the fetch operation. The macroinstruction is then executed in the microcode with the last microinstruction returning to the fetch sequence. The program counter (R_9) is incremented in order to fetch the next instruction or loaded for jump, branch, or skip instruction.

The two step buttons are used for program testing and debugging at either the macrolevel or the microlevel. If step micro is selected, each push of the step micro switch will permit one system clock pulse to increment the microinstruction address one step. In this way the microroutines may be executed on a one-step-at-a-time basis. The step macro button enables one complete fetch/execute cycle. Therefore, typical machine language programs may be executed one step at a time for program debugging purposes. The repeat button is used in conjunction with either step button or the run button as a further aid to microlevel or macrolevel testing. If step micro and repeat are selected simultaneously, the clock pulse to the 3001 microcontrol unit will be inhibited. Each time the step micro button is touched, therefore, the same microinstruction will be executed. The entire system would perform normally, with the exception of the 3001 microcontrol unit. Similarly, if repeat and step macro are selected, the increment of program counter (R_9) will be inhibited. The same microroutine will be fetched and executed each time the step macro button is touched. Since these step functions occur on a single-shot basis, they are not observable by test equipment requiring repetitive wave forms. The run button may be used in conjunction with the step repeat functions in the following manner. If either step repeat function has been selected and the run button is touched, the system will repetitively execute a single microinstruction or the same fetch/execute sequence. This permits a single microinstruction or a single microroutine to be repeated continuously. Test equipment such as oscilloscopes, waveform monitors, counters, and logic analyzers may then be used to verify proper system operation at the signal level.

RESULTS

Before the peripheral devices (magnetic tape unit, image analyzer display terminal) became available, preliminary testing demonstrated the systems ability to capture and display video images using a Fairchild CCD110 line scanner. A 1970 IEEE facsimile test chart was used as the test image during preliminary tests. The Fairchild CCD110 scanner contains only 256 pels; however, it can operate at relatively high speeds (100 nanoseconds per pel). Due to the 256-pel-per-line limit of the scanner, only a narrow stripe of the facsimile test chart could be scanned at a resolution of 200 pels per inch. Nevertheless, images were captured and displayed, and some preliminary analysis was accomplished with this setup. It has been shown with a high degree of confidence in early testing that images can be captured, stored, and processed at speeds consistent with the Postal Service's 20 pages per second goal. This, of course, is contingent on the verification that scanners can supply the required video.

In addition to simple capture and display of video images, early results include the writing, debugging, and operation of three simple processing programs. Using these programs it is possible to calculate the intensity statistics for a display image, to generate a histogram presentation of the results of the statistics generated, and to "Webervert" the displayed image from 6-bit video to 5-bit video. Verification that the operation of the system is as intended may be gained through the use of test and calibration programs.

IMAGE STATISTICS GENERATION

The image intensity statistics generator program uses an iterative approach to count the number of times each particular video intensity level exists in the display image. The output from the program is a set of 64 numbers representing the number of times each video level exists in a display.

HISTOGRAM GENERATOR

In order to present a graphic display of the results of the image statistics generation, a bar graph type display was created using the 64 intensity statistics. In the bar graph display the 64 possible intensity levels are represented by 64 horizontal bars. The bottom bar in the display represents black (or video level zero) and the top bar on the display represents white (video value 63). The length of the bar represents the number of times a particular video pel is found to exist in the displayed image. A totally black picture would generate a bar graph which would be a single bar on the bottom of the display the full length of the display and no bars for video levels 1 through 63.

Prior to generation of the bar graph itself, the statisitics data are normalized and scaled. The scale factor for a particular bar graph display is represented by a number of small black dots in the lower left hand corner of the bar graph. If there are no dots present in the display, the full scale value for a bar would be 100%. Each scale factor mark indicates that the full scale value of a bar graph has been divided by two; thus, one scale mark indicates 50% full scale, two marks indicate 25% full scale, etc. The maximum number of scale factor marks would be five, indicating a full scale value of 3.125%.

Although the original testing used the histogram generator to display image intensity statistics, the program is general purpose and could be used to present any arbitrary group of 64 numbers as a bar graph.

CALIBRATION

In order to verify that the statistics generator and histogram generator programs are operating correctly, a test input program is available for calibration purposes. This simple program generates a display of a 64-level gray scale wedge. See figure B13.* This display contains an equal number of all 64 possible gray scales. When this image is used as an input to the statistics generator, the number of pels in each gray scale should be equal to the total number of pels in the display divided by 64. The histogram resulting from such a display is shown in figure B13 (64 bars of equal length). When this set of test programs is operated (with the results indicated in fig B13), the system is verified as operating correctly.

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*The error in scale factor marks on the histogram display of figure B13 was due to incorrect settings on the display controls, not program error.

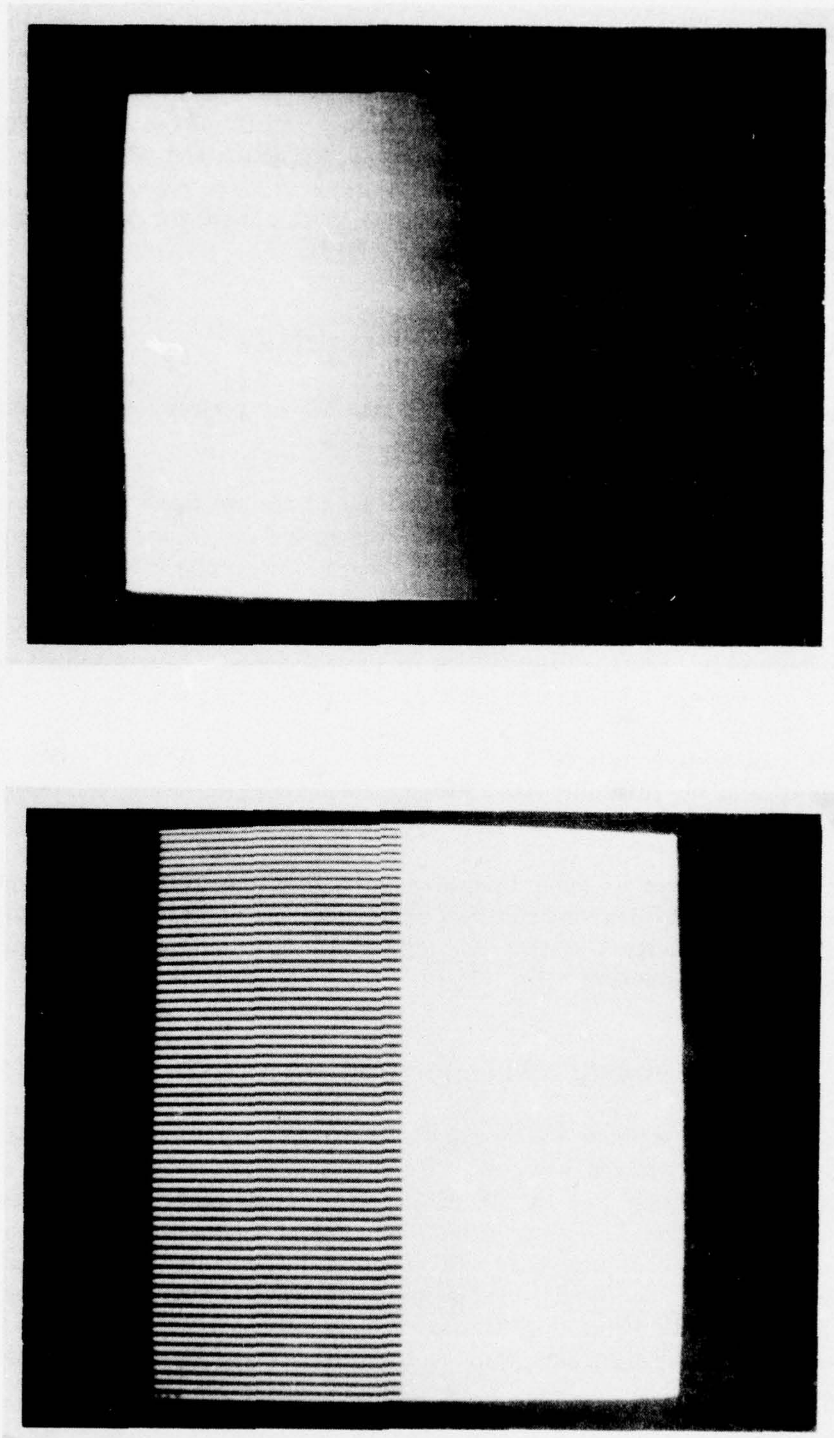


Figure B13. Program-generated test image and histogram.

TEST IMAGE

After the calibration routine indicates correct system operation, test images can be scanned and analyzed. Figure B14 is an image of a portion of the IEEE facsimile test chart and its associated histogram. As expected, this black and white image produces a histogram with two clearly identifiable concentrations of video pel values. When the Gray scale photograph portion of the facsimile test chart is used, the resulting histogram clearly does not show the bilevel behavior (see fig B15).

CONCLUSIONS AND SUMMARY

1. The frame store memory and memory controller are performing all the operations required by the design goals.

2. Speed of operation of 10.5 megapels per second has not quite been met. Data can be accommodated safely to about 9.6 megapels per second. The cause of the limitation is known and can be corrected in the equipment if and when a 10.5 megapel per second data rate is needed.

3. The method of expanding the system to control eight frame store memories rather than one is a low-risk engineering design augmentation.

4. The successful operation of the frame store memory and memory controller demonstrates the feasibility of capturing, storing, and buffering high-resolution image data at the required 20 pages per second data rate.

5. The compression of 64 linear brightness levels to 32 logarithmic levels and the generation of pel brightness statistics and histograms by the memory controller under software program control demonstrate the flexibility and processing power of the equipment.

PLANNED NELC FUTURE ACTIVITIES

The frame store memory and its controller will be used as a principal part of a video image acquisition, storage, and processing system. There are a number of ongoing activities which will be supported by the image acquisition system. These include support of solid-state scanning device testing, the gathering and analysis of image statistics, the evaluation of techniques potentially useful in image compression and enhancement, as well as others. The frame store memory, its controller, and the associated peripheral hardware will provide the necessary vehicle by which the applicability of scanning devices and processing algorithms to high-speed image capture and transmission can be determined.

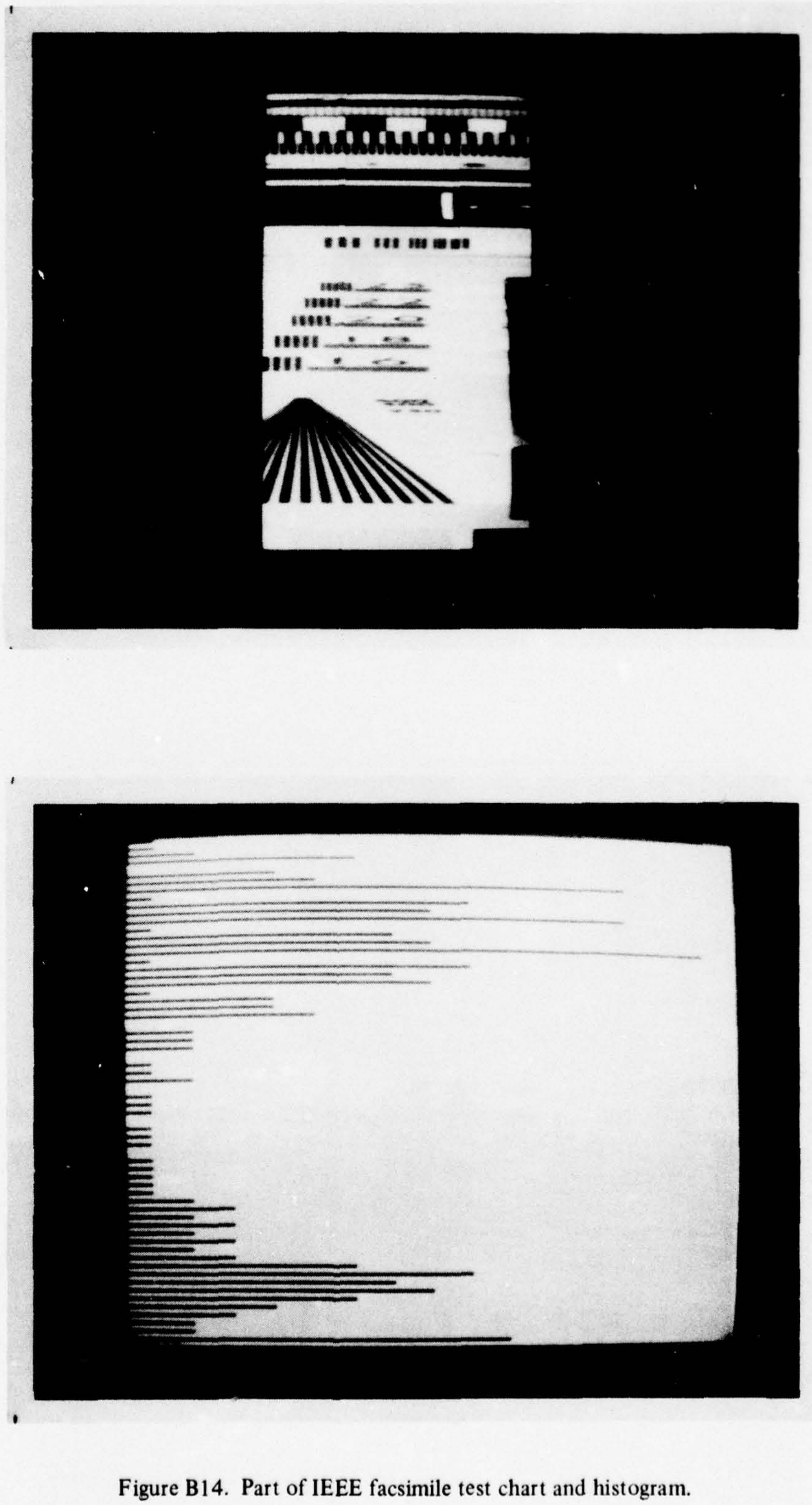


Figure B14. Part of IEEE facsimile test chart and histogram.

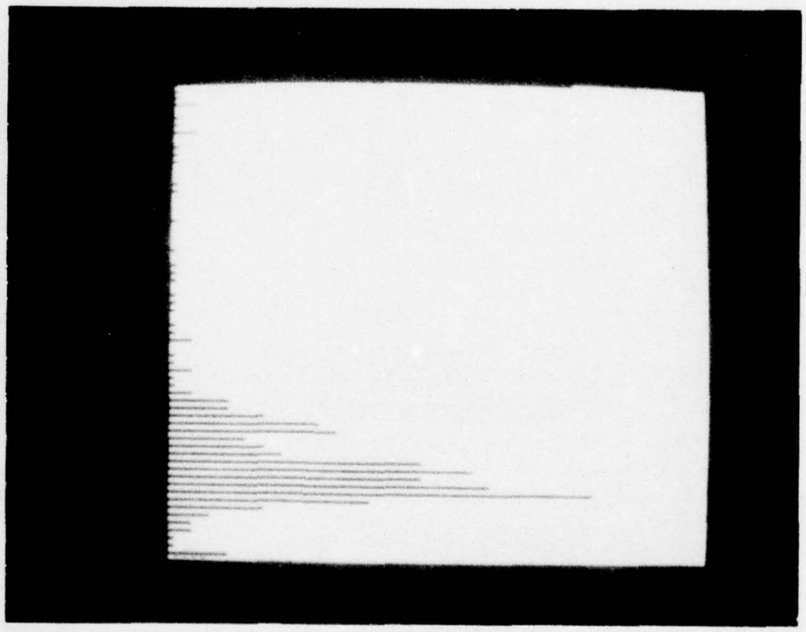


Figure B15. Part of IEEE facsimile test chart and histogram (gray scale).

SOLID-STATE SCANNER TESTING

The memory and controller will be used on a continuing basis to support the detailed testing, characterization, analysis, and development of solid-state image scanners. Both area and line arrays will be evaluated. The supporting hardware and interfaces are sufficiently versatile to allow continued support of the scanner testing effort. Results gained in early testing with the CCD110 256-pel scanner will be amplified by installing a 1728-pel line scanner (the Fairchild CCD121). Subsequently to the evaluation of the long linear scanner, an area device will be installed in image tracking mode and evaluated.

STATISTICAL DATA ACQUISITION AND PROCESSING

Once the electro-optical characteristics of scanning devices have been tested and characterized, the devices will be used as image acquisition sensors to acquire complete 8 1/2-by-ll-inch video images. These images will be stored on magnetic tape in digital form for further processing. The memory controller and its peripheral hardware will compute a wide variety of image statistics using the images scanned by solid-state scanners and stored on magnetic tape. The image statistics will be presented in both tabular and graphical form to aid the characterization of image types. Examples are the image intensity statistics and associated bar graphs in figures B13, B14, and B15. More complicated types of statistics or perhaps combinations of statistics may be used to evaluate processing algorithms for the purpose of dynamically controlling the analog scanning hardware.

ENHANCEMENT AND COMPRESSION TECHNIQUES

The processed statistical data may be used to predict the compressibility of the video image. An attempt will be made using the statistical data and perhaps other processes to predict whether or not a particular type of image is compressible or enhanceable. Various compression and enhancement algorithms may be tested to determine the accuracy of predictions.

SPECIFIC TASKS

1. Interface with the Kennedy Tape Transport which is due at the end of May.

2. Continue to improve the supervisory software controls so that such commands as CLEAR, LOAD PROGRAM (S), CAPTURE, ANALYZE (with options), DISPLAY IMAGE, DISPLAY TABULAR STATISTICS, PRINT TABULAR STATISTICS, DISPLAY GRAPHIC STATISTICS, PRINT GRAPHIC STATISTICS (at low resolution), READ IMAGE FROM TAPE, etc, are simple one- or two-pushbutton commands.

3. When a well defined procedure for analysis is established in June, connect the macroprograms above in sequences for rapid acquisition of image test data.

4. Consider the acquisition of a second frame store memory module (about $20k material cost) to verify the expansion capability and logic design.

5. Consider modification of packing and unpacking logic to allow program control of number of bits accepted per video pel word.

6. Implement a program to store images on magnetic tape in a format which is compatible with facilities capable of producing full 8 1/2-by-11-inch high-resolution prints. Potential sources are the Image Processing Institute at USC in Los Angeles; and Perkin Elmer Company in Pasadena, California.

APPENDIX A (TO TR 2020 APPENDIX B): MICROPROGRAMMING

MICRO INSTRUCTION FIELD DECODE

Field	μ-word bits	Code (Binary)	Function
AC	06-00	–	See 3001 data sheet (next address)
FC	10-07	–	See 3001 data sheet (flag control)
F	17-11	–	See 3002 data sheet (function code)
K	19-18	0 0	K = all zeros
		0 1	K = K_x*
		1 0	
		1 1	K = all ones
MDB enables	22-20	0 0 0	NOP
		0 0 1	AC → MDB
		0 1 0	
		0 1 1	
		1 0 0	
		1 0 1	
		1 1 0	
		1 1 1	SDB → MDB
SDB enables	25-23	0 0 0	NOP
		0 0 1	Memory → SDB
		0 1 0	Input Logic → SDB
		0 1 1	Aux I/O → SDB
		1 0 0	Data Switches → SDB
		1 0 1	
		1 1 0	
		1 1 1	MDB → SDB
Memory Control	27-26	0 0	NOP
		0 1	WRITE
		1 0	READ
		1 1	REFRESH REQUEST
Clock Control	29-28	0 0	NOP
		0 1	Set HS Clk-Enable TTL μm
		1 1	Set MS Clk-Enable MOS μm
		1 0	Set EX Clk-Enable TTL μm

* x specified by EFB_{1-10}

Field	μ-word bits	Code (binary)	Function
CK INH	30	0	NOP
		1	Inhibit CPE clock
External Function A	34-31	0 0 0 0	NOP
		0 0 0 1	Set "Step Macro"
		0 0 1 0	Capture
		0 0 1 1	
		0 1 0 0	
		0 1 0 1	Clear Front Panel
		0 1 1 0	IR (R_n)
		0 1 1 1	IR ($Sense_n$)
		1 0 0 0	Vertical Sync
		1 0 0 1	IR (K_n)
		1 0 1 0	I/O Strobe (IOS)
		1 0 1 1	
		1 1 0 0	
		1 1 0 1	
		1 1 1 0	
		1 1 1 1	
External Function B	38-35	0 0 0 0	NOP
		0 0 0 1	Display Cycle Start (DCS)
		0 0 1 0	SPX - MDB
		0 0 1 1	N → FO, 3 (N)
		0 1 0 0	SPX → IR
		0 1 0 1	Memory Protect (M PROT)
		0 1 1 0	Data available out (DAO)
		0 1 1 1	Boot TAPE
		1 0 0 0	Horizontal sync
		1 0 0 1	Data Ready for TAPE (DRT)
		1 0 1 0	
		1 0 1 1	
		1 1 0 0	
		1 1 0 1	
		1 1 1 0	
		1 1 1 1	

Field	μ-word bits	Code (binary)	Function	
MARB	40-39	0 0	NOP	
		0 1		
		1 0	MAR → MARB	
		1 1	MDB → MARB	(MDBM)
TEST ENABLE	45-41	0 0 0 0 0	CO/RO	
		0 0 0 0 1	SENSE 1	
		0 0 0 1 0	SENSE 2	
		0 0 0 1 1	SENSE 3	
		0 0 1 0 0	SENSE 4	
		0 0 1 0 1	SENSE 5	
		0 0 1 1 0	SCANNER DA	(DA)
		0 0 1 1 1	MAN FI	
		0 1 0 0 0	TRUE	
		0 1 0 0 1	MDB_{47}	
		0 1 0 1 0	RUN	
		0 1 0 1 1	Flag out	
		0 1 1 0 0	LINE SYNC (Scanner)	(LS)
		0 1 1 0 1	R_n	
		0 1 1 1 0	DSR_{24}	
		0 1 1 1 1	MDB_0	
		1 0 0 0 0	I/O status	
		1 0 0 0 1	WAIT (tape)	
		1 0 0 1 0	Tape gap detected	(TGD)
		1 0 0 1 1	Read data strobe	(RDS)
		1 0 1 0 0		
		1 0 1 0 1		
		1 0 1 1 0		
		1 0 1 1 1		
		1 1 0 0 0		
		1 1 0 0 1		
		1 1 0 1 0		
		1 1 0 1 1		
		1 1 1 0 0		
		1 1 1 0 1		
		1 1 1 1 0		
		1 1 1 1 1		

MACRO INSTRUCTION SUMMARY

OP CODE	MNEMONIC	FUNCTION		OP CODE	MNEMONIC	FUNCTION
200	LDA	Load A		240	SRO	Shift A right, 1 fill
201	LDAX (x)	Load A indexed		241	SRZ	Shift A right, 0 fill
202	STA	Store A		242	SLZ	Shift A left, 0 fill
203	STAX (x)	Store A indexed		243	SRC	Shift A right, circular
204	LDX (x)	Load index		244	AND	Logical AND
205	STX (x)	Store index		245	IOR	Logical OR
206	LSP	Load stack pointer		246	XOR	Logical XOR
207	LDK (x)	Load K-register		247	COM	Complement
210	CAPT	Capture		250	ADD	Add A
211	CLX (x)	Clear index		251	SUB	Subtract A
212	INX (x)	Increment index		252	INC	Increment A
213	DXC (x)	Decrement index		253	DEC	Decrement A
214	DSZ (x)	DCX, skip 0 result		254	CLA	Clear A
215	DISP	DISPLAY		255		
216	HALT	HALT		256	SMC	Set MOS Clock
217	NOP	Null operation		257		
220	JP	Jump unconditional		260	MPR (Y)	Memory Protect
221				261	TRAX (x)	Transfer (A) to index
222				262	TRXA (x)	Transfer (index) to A
223	JNN	Jump A $\geq$ O		263	PUSH	(A) placed on TOS
224	JPN	Jump A $<$ O		264	POP	(TOS) placed in A
225	JPZ	JUMP A = O		265	LDAC	Load A with contant
226	JNZ	Jump A = O		266	ADDC	Add constant to A
227				267	SUBC	Subtract constant from A
230				270	CAPL	Capture Line
231	JPX (x)	Jump indexed		271	OUTV (x)	Output Video on ch x
232	JPA	Jump A		272		
233	BYT	Shift right 8 bits		273	INPT (x)	Input from tape ch x
234	JPI	Jump indirect		274	OUTT (x)	Output to tape ch x
235	JPR	Jump subroutine return		275	INP (x)	Input on ch x
236	JSR	Jump to subroutine		276	OUT (x)	Output on ch x
*237	SKIP	Skip on Skip x set		277	SIOC (x)	Skip on I/O cond.

(x) indicates modifier sensitive

* not yet implemented

TOS = top of stack

PROGRAMMING NOTES

1) R_6 and R_7 contents are altered during the course of certain instructions.

2) Before executing a program, stack pointer, R_8 should be set to desired first stack location.

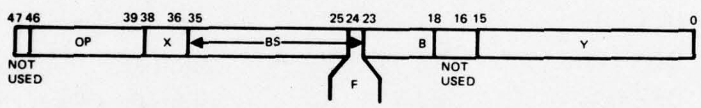
3) All arithmetic and logical instructions leave the result in the accumulator.

4) Interrupt sequence assumes handling routine to be resident at location 0 in program storage.

5) Memory protect is program-accessible only in that it protects those portions of memory designated by front panel switches on invocation of MPR instruction. Unless this effect is required, MPR should be used only from front panel. Memory protect does not protect against loss of refresh or loss of power.

6. Any interrupt handling routine must end with POP and JPR to restore to entry conditions.

MACRO INSTRUCTION FORMAT



( )	=	contents of
→	=	Replaces contents of
AT	=	AC and T
jump	=	transfer program control

A	=	accumulator
R_x	=	index register x
Y	=	address or constant
P	=	program address register (R_9)
S	=	stack pointer (R_8)
SK_x	=	Skip X
A_i	=	accumulator bit i
B_s	=	buffer size
F	=	Front panel fetch
B	=	Byte Select
/B/	=	Byte Select Inputs (octal)

MACRO INSTRUCTIONS

OP $CODE_8$	MNEMONIC	FUNCTION	DESCRIPTION
200	LDA	$(Y) \rightarrow A$	Load accumulator
201	LDSX (x)	$(R_X + Y) \rightarrow A$	Load acc. with contents of $R_X + Y$
202	STA	$A \rightarrow Y$	Store contents of act in memory location Y
203	STAX (x)	$A \rightarrow Y + R_X$	Store contents of ace in memory location ($Y - R_X$
204	LDX (x)	$(Y) \rightarrow R_X$	Load index R_X with contents of Y
205	STX (x)	$R_X \rightarrow Y$	Store contents of R_X in memory location Y
206	LSP	$(Y) \rightarrow S$	Load stack pointer with stack beginning location
207	LDK (x)	$(Y) \rightarrow K_X$	Load K_X
210	CAPT		Initiate capture routine in TTL Roms
211	CLX (x)	$O \rightarrow R_X$	Clear index R_X
212	INX (x)	$R_X + 1 \rightarrow R_X$	Add 1 to contents of R_X
213	DCX (x)	$R_X - 1 \rightarrow R_X$	Subtract 1 from contents of R_X
214	DSZ (x)	$R_X - 1 \rightarrow R_X$ $P + 1 \rightarrow P$	Subtract 1 from contents of R_X skip the following instruction
215	DISP		Initiate the DISPLAY routine in TTL Roms
216	HALT		Sets STEP MACRO and stops MCU clock
217	NOP		No operation
220	JP	$Y \rightarrow P$	Transfer program control to location Y
221			
222			
223	JNN	if $A \geqslant O$ $Y \rightarrow P$	If contents of accumulator is not negative ($\geqslant$O) then jump to Y
224	JPN	if $A < O$	If contents of accumulator is negative (<O) then jump to Y
225	JPZ	if $A = O$ $Y \rightarrow P$	If contents of accumulator is zero then jump to Y

OP CODE$_8$	MNEMONIC	FUNCTION	DESCRIPTION
226	JNZ	if $A \neq O$ $Y \rightarrow P$	If contents of accumulator is not zero then jump to Y
227			
230			
231	JPX (x)	$R_x + Y \rightarrow P$	Jump to location specified by sum of the contents of R_x and Y
232	JPA	$A \rightarrow P$	Jump to location specified by the contents of the accumulator
233	BYT	$A_i \rightarrow A_{i-8}$ (mod$_{47}$)	Shift accumulator right 8 bits
234	JPI	$(Y) \rightarrow P$	Jump to location specified by the contents of Y
235	JPR	$((S)) \rightarrow P$ $(S) - 1 \rightarrow S$	Jump to location specified by the stack pointer s subtract 1 from the contents of s
236	JSR	$P \rightarrow (S)$ $Y \rightarrow P$	Store next instruction location on top of stack specified by contents of S jump to Y
*237	SKIP	if SK_x $P + 1 \rightarrow P$	If skip x has been set the skip following instr.
240	SRO	$A_i \rightarrow A_{i-Y}$ $1 \rightarrow A_{47} - A_{47-Y}$	Shift contents of accumulator right Y bits and fill left end of accumulator with 1's
241	SRZ	$A_i \rightarrow A_{i-Y}$ $O \rightarrow A_{47}$-A_{47-Y}	Shift contents of accumulator right Y bits and fill left end of accumulator with O's
242	SLZ	$A_i \rightarrow A_{i+Y}$ $O \rightarrow A_o - A_{Y-1}$	Shift contents of accumulator left Y bits and fill right end of accumulator with O's
243	SRC	$A_i \rightarrow A_{i-Y}$ mod$_{47}$	Shift contents of accumulator right Y bits and fill left end of accumulator with the Y bits shifted off right end
244	AND	$A \wedge (Y) \rightarrow A$	Logically AND the contents of the accumulator with the contents of Y
245	IOR	$A \vee (Y) \rightarrow A$	Logically OR the contents of the accumulator with the contents of Y
246	XOR	$A + (Y) \rightarrow A$	Logical exclusive-or of the contents of the accumul and the contents of Y

OP $CODE_8$	MNEMONIC	FUNCTION	DESCRIPTION
247	COM	$A \rightarrow A$	Logically complement the contents of the accumulator
250	ADD	$A + (Y) \rightarrow A$	Add the contents of Y to the contents of the accumulator
251	SUB	$A - (Y) \rightarrow A$	Subtract the contents of Y from the contents of the accumulator, leaving a 2's-complement result
252	INC	$A + 1 \rightarrow A$	Add one to the contents of the accumulator
253	DEC	$A - 1 \rightarrow A$	Subtract one from the contents of the accumulator
254	CLA	$0 \rightarrow A$	Set the contents of the accumulator to zero
255			
256	SMC		Set MOS clock
257			
260	MPR (Y)	Y → MP Register	The individual 16ths (4k) of main memory for which those bits in Y are set are write disabled
261	TRAX (x)	$A \rightarrow R_x$	Contents of accumulator are copied into index
262	TRXA (x)	$R_x \rightarrow A$	Contents of index are copied into accumulator
263	PUSH	$A \rightarrow (S)$ $S + 1 \rightarrow S$	Contents of accumulator are copied onto top of stack and stack pointer is incremented
264	POP	$((S)) \rightarrow A$ $S - 1 \rightarrow S$	Contents of top of stack are copied into accumulator and stack pointer is decremented
265	LDAC	$Y \rightarrow A$	Load Y into accumulator
266	ADDC	$A + Y \rightarrow A$	Add Y to accumulator
267	SUBC	$A - Y \rightarrow A$	Subtract Y from accumulator
270	CAPL	Capture line	Capture one line from the video scanner for the number of words specified by the contents of R_7 and store at address specified by Y

OP $CODE_8$	MNEMONIC	FUNCTION	DESCRIPTION
271	OUTV (x)	Output video	Place one video record on tape channel x, beginning at location Y in memory, and continuing for the number of words specified by the contents of R_6. Requires the constant 7 to be in R_2 and 77 to be in K_3.
272			
273	INPT (x)	Read tape buffer	Transfer the record immediately following current position from tape on channel x to a buffer beginning at location Y.
274	OUTT (x)	Write tape buffer	Transfer the contents of a buffer beginning at location Y and ending at location Y + S – 1 to tape on channel x
275	INP (x)	$(I/\emptyset\ ch)_x \rightarrow Y$	Input one word on I/O channel x to memory location Y
276	OUT (x)	$(Y) \rightarrow I/O\ ch_x$	Output one word from memory location Y on I/O channel x
277	SIOC (x)	Skip on I/O condition	If I/O condition x is met, then skip next instruction (see table 2 on following page)

table 1: I/O channels

x	device
0	none
1	CRT Terminal
2	Tape 1 (Bright)
3	
4	
5	Video analyzer
6	Tape 2 (Kennedy)
7	

table 2: SIOC functions

x	function
0	none (skip always)
1	TERMINAL DATA READY
2	TERMINAL BUSY
3	File Mark (Bright Tape)
4	Scanner Data Available
5	
6	
7	

AUXILIARY OP CODES

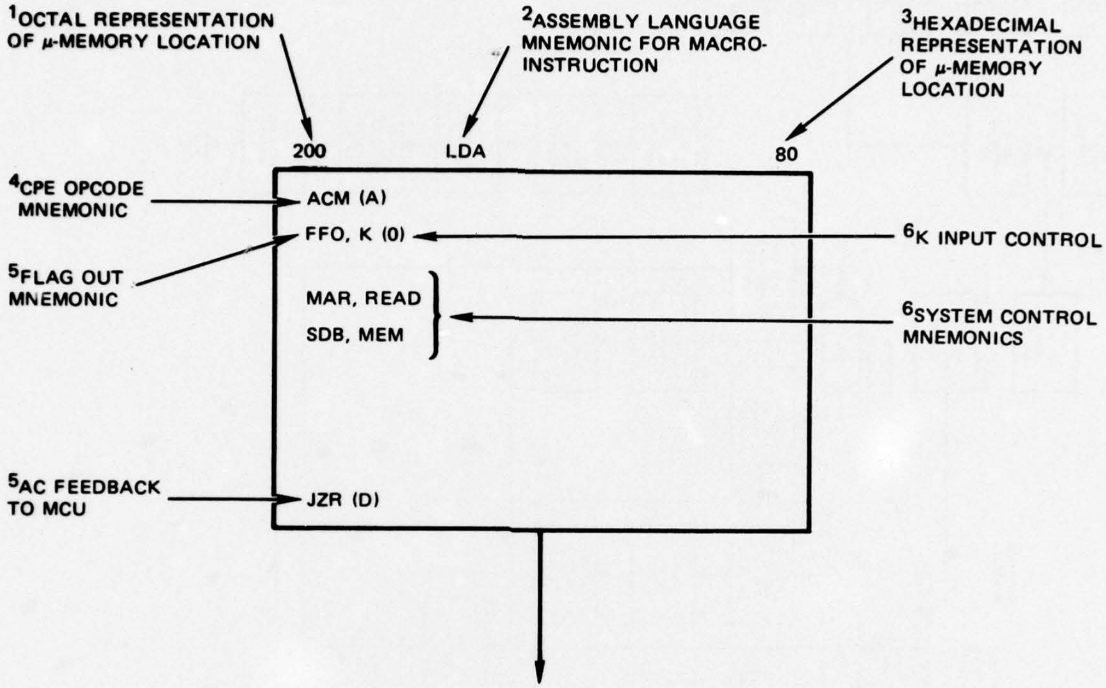
(those routines not normally recognized as op codes but which may be used as such)

OPCODE	FUNCTION	COMMENTS
006	EXAMINE	$Y \rightarrow R_7$; $((R_7)) \rightarrow$ Display
007	EXAMINE NEXT	$R_7 + 1 \rightarrow R_7$; $((R_7)) \rightarrow$ Display
017	FETCH	
030	DEPOSIT	(FP)* $\rightarrow (R_7)$; Examine Next
135	SET AC	(FP) $\rightarrow$ A
137	SET R_n	(FP) $\rightarrow R_n$**
175	DISPLAY AC	(A) $\rightarrow$ Display
177	DISPLAY R_A	(R_n)** $\rightarrow$ Display
000	FAULT	
360	BOOT	
377	INTERRUPT	

* FP = front panel data switches

** n is 10-digit lever switch; Acc value is lost when used in this mode

ROM FLOWCHART FORMAT



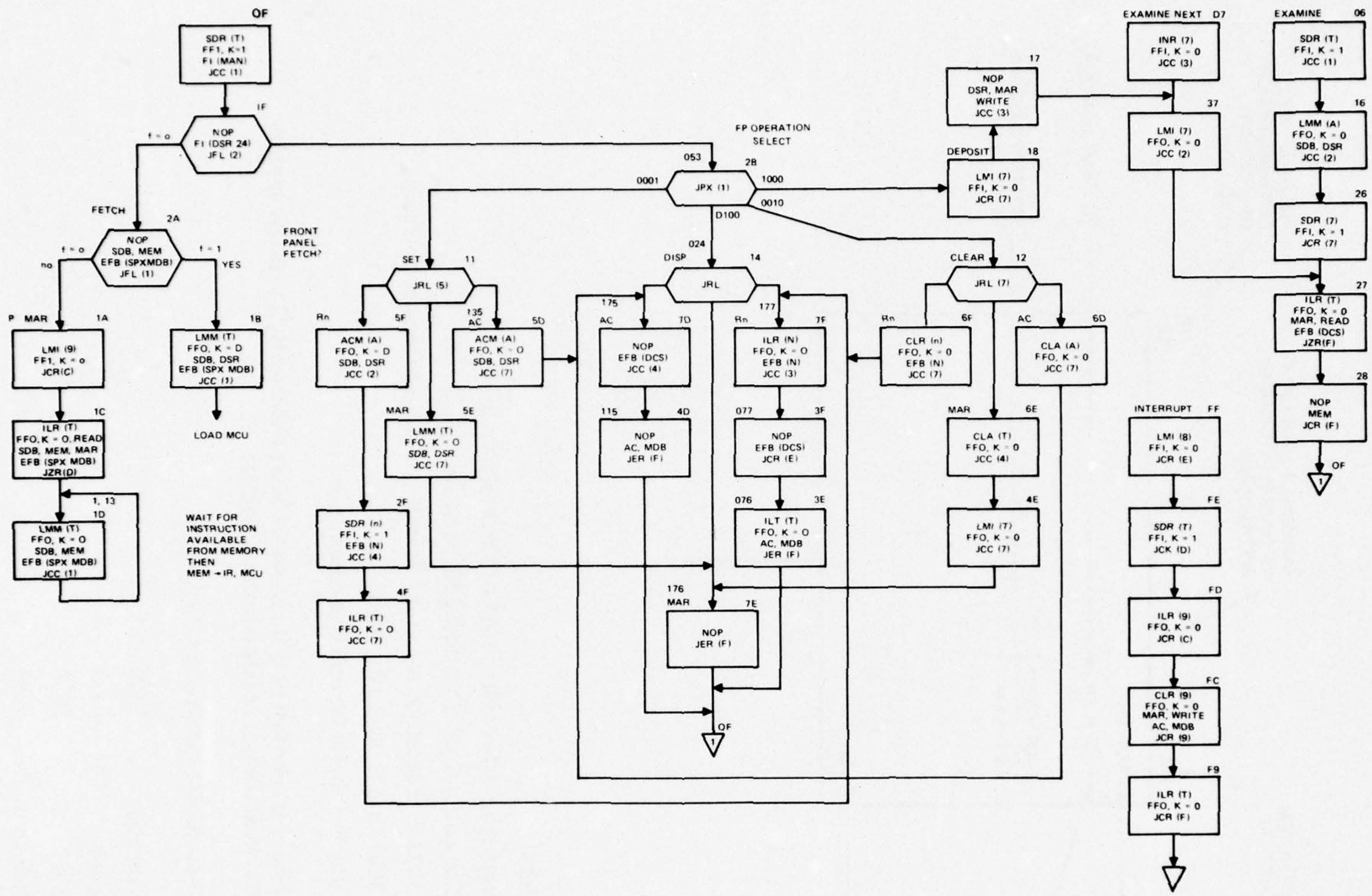
notes:

1. optional
2. appears only at first microword of a macroinstruction
3. leading zero not given for first 256 locations
4. see 3002 data sheet for function. Parentheses indicate register operated on
5. see 3001 data sheet for function
6. see attached sheets for function description

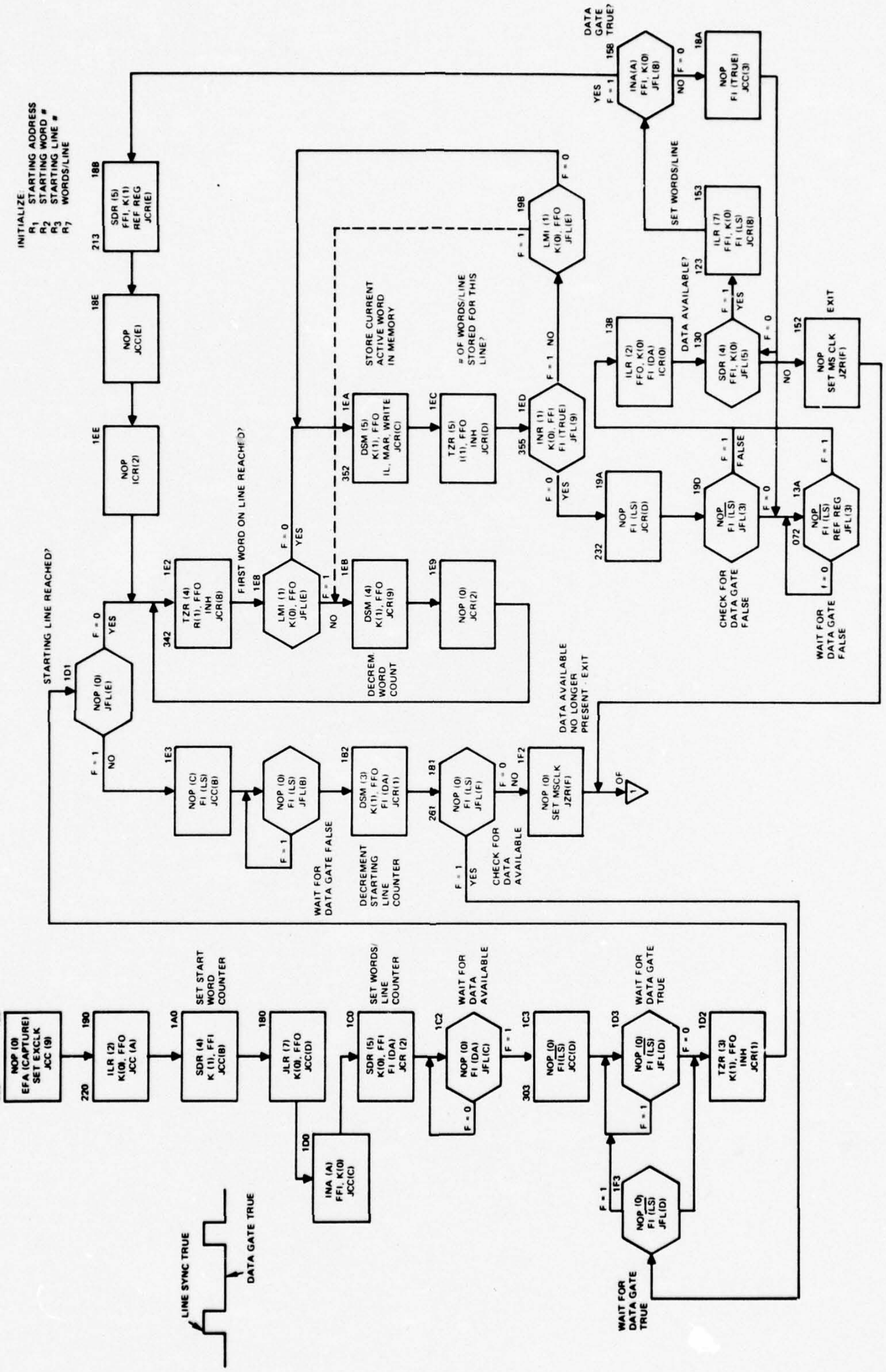
A. Flag input is specified only if not the default condition HCZ and then appears with system control or flag out and K-control.

Default conditions (if not specified on flowchart)

CPE op code	–	NOP
Flag out	–	FFO
Flag in	–	HCZ
System cont.	–	none
Test mux	–	CO/RO - true value



OF
SDR (T) FF1, K=1 FI (MAN) JCC (1)
1F
NOP FI (DSR 24) JFL (2)
f = o
FETCH
2A
NOP SDB, MEM EFB (SPXMDB) JFL (1)
f = o
no
f = 1
YES
FRONT PANEL FETCH?
P MAR
1A
LMI (9) FF1, K = o JCR(C)
1C
ILR (T) FFO, K = O, READ SDB, MEM, MAR EFB (SPX MDB) JZR(D)
1, 13
1D
LMM (T) FFO, K = O SDB, MEM EFB (SPX MDB) JCC (1)
1B
LMM (T) FFO, K = D SDB, DSR EFB (SPX MDB) JCC (1)
LOAD MCU
WAIT FOR INSTRUCTION AVAILABLE FROM MEMORY THEN MEM → IR, MCU
FP OPERATION SELECT
053
2B
JPX (1)
0001
1000
0010
D100
SET
11
JRL (5)
Rn
5F
ACM (A) FFO, K = D SDB, DSR JCC (2)
135 AC
5D
ACM (A) FFO, K = O SDB, DSR JCC (7)
MAR
5E
LMM (T) FFO, K = O SDB, DSR JCC (7)
2F
SDR (n) FFI, K = 1 EFB (N) JCC (4)
4F
ILR (T) FFO, K = O JCC (7)
024
DISP
14
JRL
175
AC
7D
NOP EFB (DCS) JCC (4)
115
4D
NOP AC, MDB JER (F)
Rn
177
7F
ILR (N) FFO, K = O EFB (N) JCC (3)
077
3F
NOP EFB (DCS) JCR (E)
076
3E
ILT (T) FFO, K = O AC, MDB JER (F)
176
MAR
7E
NOP JER (F)
OF
1
CLEAR
12
JRL (7)
Rn
6F
CLR (n) FFO, K = 0 EFB (N) JCC (7)
AC
6D
CLA (A) FFO, K = 0 JCC (7)
MAR
6E
CLA (T) FFO, K = 0 JCC (4)
4E
LMI (7) FFO, K = 0 JCC (7)
DEPOSIT
18
LMI (7) FFI, K = 0 JCR (7)
17
NOP DSR, MAR WRITE JCC (3)
EXAMINE NEXT D7
INR (7) FFI, K = 0 JCC (3)
37
LMI (7) FFO, K = 0 JCC (2)
EXAMINE 06
SDR (T) FFI, K = 1 JCC (1)
16
LMM (A) FFO, K = 0 SDB, DSR JCC (2)
26
SDR (7) FFI, K = 1 JCR (7)
27
ILR (T) FFO, K = 0 MAR, READ EFB (DCS) JZR(F)
28
NOP MEM JCR (F)
OF
1
INTERRUPT FF
LMI (8) FFI, K = 0 JCR (E)
FE
SDR (T) FFI, K = 1 JCK (D)
FD
ILR (9) FFO, K = 0 JCR (C)
FC
CLR (9) FFO, K = 0 MAR, WRITE AC, MDB JCR (9)
F9
ILR (T) FFO, K = 0 JCR (F)



INITIALIZE:
R1 STARTING ADDRESS
R2 STARTING WORD #
R3 STARTING LINE #
R7 WORDS/LINE
LINE SYNC TRUE
DATA GATE TRUE
SET START WORD COUNTER
SET WORDS/LINE COUNTER
WAIT FOR DATA AVAILABLE
WAIT FOR DATA GATE TRUE
STARTING LINE REACHED?
FIRST WORD ON LINE REACHED?
STORE CURRENT ACTIVE WORD IN MEMORY
OF WORDS/LINE STORED FOR THIS LINE?
DECREM WORD COUNT
WAIT FOR DATA GATE FALSE
DECREMENT STARTING LINE COUNTER
CHECK FOR DATA AVAILABLE
DATA AVAILABLE NO LONGER PRESENT - EXIT
DATA AVAILABLE?
SET WORDS/LINE
DATA GATE TRUE?
CHECK FOR DATA GATE FALSE
WAIT FOR DATA GATE FALSE
EXIT

APPENDIX C: ADVANCED IMAGER

Prepared

for

US POSTAL SERVICE

June 1976

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INTRODUCTION

This report contains data on scanning devices, the test beds, and illumination sources generated since the first anniversary date of the program, 22 October 1975. Since that date there have been no new off-the-shelf candidate imaging devices from any of the major suppliers which are directly applicable to the USPS requirements.

Consequently, NELC, with the approval of the USPS Design Division, has initiated a contract with RCA, Princeton, which if successful will provide design data for a solid-state imaging device meeting all the USPS imaging goals. Actual test devices which are somewhat smaller in area will be fabricated, evaluated, and submitted to NELC for further tests. The general goals of this contract are contained in the body of this report. The proprietary details of the contracted work are contained in TR 2020 Volume 2, distribution of which is limited to US Government agencies.

During this program year an entirely new large drum test bed has been fabricated and operated, and is integrated into the total aquisition system. A new method of illumination has been added which utilizes flourescent tubes rather than an incandescent source. A 1728-pel imager has been integrated into the system in order to accommodate full 8½-inch copy width acquisition.

Test plans have been formulated for the calibration of the system and the acquisition of full-page data for the data compression-study which will begin almost immediately. This report contains the detailed techniques and calculations of lens distances, illumination correction methods, area scanner aberrations, and the plan to utilize them.

RELEVANCE TO DoD MISSION

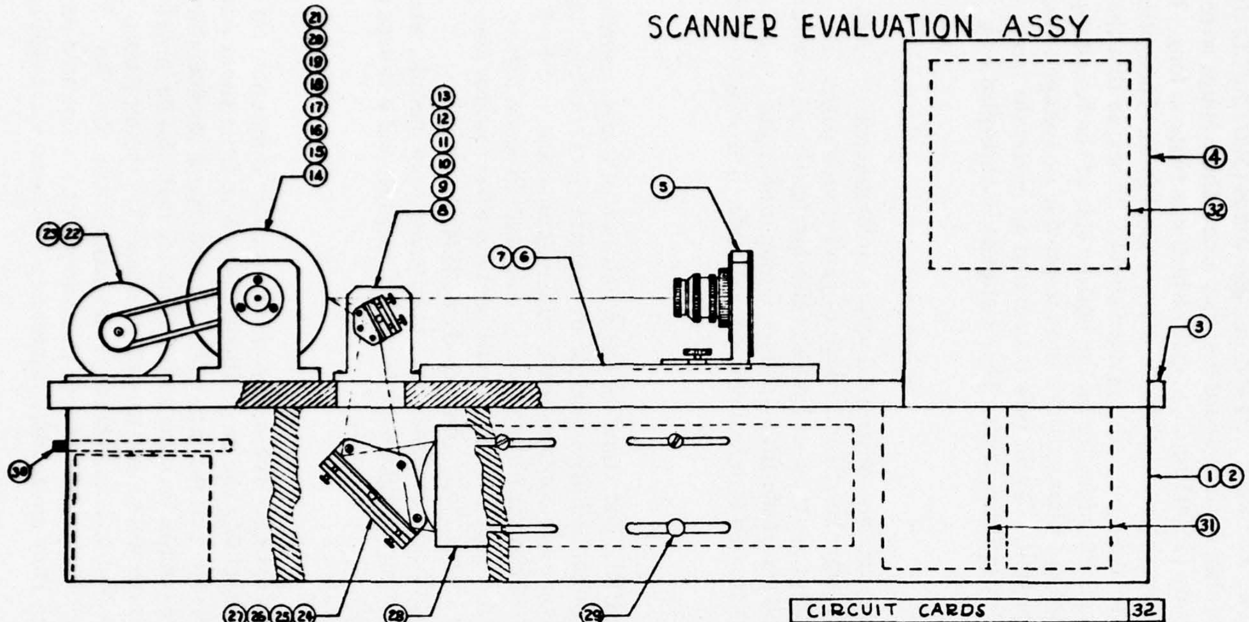
There are many similarities between USPS imaging goals and some desired military objectives. In the USPS concept, the imager remains at rest while the "targets," the pages of copy, move rapidly past the field of view. Land-based military applications may utilize the same approach for battlefield surveillance or intrusion detection. The greater military interest appears to lie where the sensor is in motion (and perhaps the target). The most likely airborne applications are teleguidance and telereconnaissance. A "tracking" imaging device such as the one being developed at RCA laboratories will offer some definite design advantages to systems in which relative motion exists between the imaging system and the target.

DRUM SCANNER TEST BEDS

SMALL DRUM TEST BED

PHYSICAL DESCRIPTION

The small drum test bed (SDTB) was built for dynamically evaluating line scanner devices and to provide input data for the image analyzer and frame store memory. Figure C1 shows most of the major components. Each major part is described briefly in the following paragraphs.



				CIRCUIT CARDS	32
				POWER SUPPLIES	31
MIRROR BACKING PLATE (A)	10	BEARING END CAP (LH)	20	LIGHT SOURCE BRIGHTNESS ADJ	30
MIRROR MOUNTING BRKT (LH) (A)	9	BEARING END CAP (RH)	19	LIGHT SOURCE ADJ KNOB	29
MIRROR MOUNTING BRKT (RH) (A)	8	DRUM MOUNTING BRKT (LH)	18	LIGHT SOURCE	28
SCANNER ADJ. GUIDE (LH)	7	DRUM MOUNTING BRKT (RH)	17	MIRROR (B)	27
SCANNER ADJ. GUIDE (RH)	6	DRUM END PLATE (LH)	16	MIRROR BACKING PLATE (B)	26
LENS-SCANNER ASSY	5	DRUM END PLATE (RH)	15	MIRROR ADJ MOUNT (LH) (B)	25
CIRCUIT BOARD ENCLOSURE	4	DRUM	14	MIRROR ADJ MOUNT (RH) (B)	24
SCANNER OPTICAL BENCH	3	MIRROR (A)	13	MOTOR MOUNTING PLATE	23
BENCH SUPPORT (LH)	2	MIRROR ADJ MOUNT (LH) (A)	12	MOTOR	22
BENCH SUPPORT (RH)	1	MIRROR ADJ MOUNT (RH) (A)	11	DRUM SHAFT	21

Figure C1. Small drum test bed.

SCANNER BENCH. This part consists of a 14-by-32-by3/4-inch plate serving as the bench top and two 5-by-31-by-1/2-inch rails used as legs for the bench. These three parts weigh about 45 pounds, making a good stable platform for the other components.

ILLUMINATION SOURCE. A Dest Data projector is used for the illumination source. As originally built, it used two 500-watt, 120-volt halogen lamps (500T30/CL/U) mounted end to end to give a line of illumination about 8 inches long. These lamps were replaced with one 1500-W, 240-V lamp (1500T30/CL/U-240) which was twice as long. The projector focused the light about 3 inches from the source in its original form. The optical path of the projector was modified to make the focal distance about 9 inches, so that there is adequate working distance to mount the projector on the bottom side of the bench top. The projector also contains a rectifier and filter network so as to provide dc voltage to the lamps and a "muffin" fan to cool the unit. The air flow is such that air enters the lamp housing at one end of the lamp and exits at the other. The brightness is controlled by a 10-ampere Variac.

DRUM AND MOTOR. The drum was constructed with a circumference of 12 inches, which allowed for 11 inches of paper length and 1 inch of gap between pages. The motor, an 1800-rpm hysteresis synchronous type, and pulleys give lps (letters per second) rates of 20, 10, and 5. The drive belt was made from 1/8-inch O-ring rubber glued together with Eastman cement. The bearings are of a standard commercial grade. The weight of the drum is about 11 pounds.

CIRCUIT BOARD ENCLOSURE. Data flow for the acquisition of images using CCD arrays is shown in figure C2. The scanner and drive module are mounted immediately behind the lens assembly. The electronics enclosure contains five modules approximately 5-by-5-inches on a side. These cards are similar to the Navy Standard Hardware Program (SHP) modules except that they are twice the height. Each module contains 80 connector pins and is compatible with the Navy present standard electronic module (SEM) program.

The five modules in the circuit board enclosure are: sample and hold module, analog-to-digital converter module, input/output module, scanner control module, and a voltage regulator module (not shown in fig C2).

SCANNER AND DRIVER MODULE. The solid-state line scanner is mounted on the lens-scanner assembly (fig C3). This assembly can be positioned anywhere from about 6 to 24 inches from the drum. This allows the pels per inch to be adjusted over a considerable range. Some lenses used do not have built-in focusing so the assembly may also be moved for fine focus adjustment. Adapter rings were made to accommodate "C" mount lenses, a Nikon bayonet adapter ring, and a 30-mm/1-mm thread for a special Nikon copy lens. The line scanner, its immediate drive circuitry, and the output video amplifier are mounted on the back side of the scanner module. They are actually fastened to a micarta board that can

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Metrication information: 1 in = 25.4 mm
1 lb = 0.45 kg (approx)

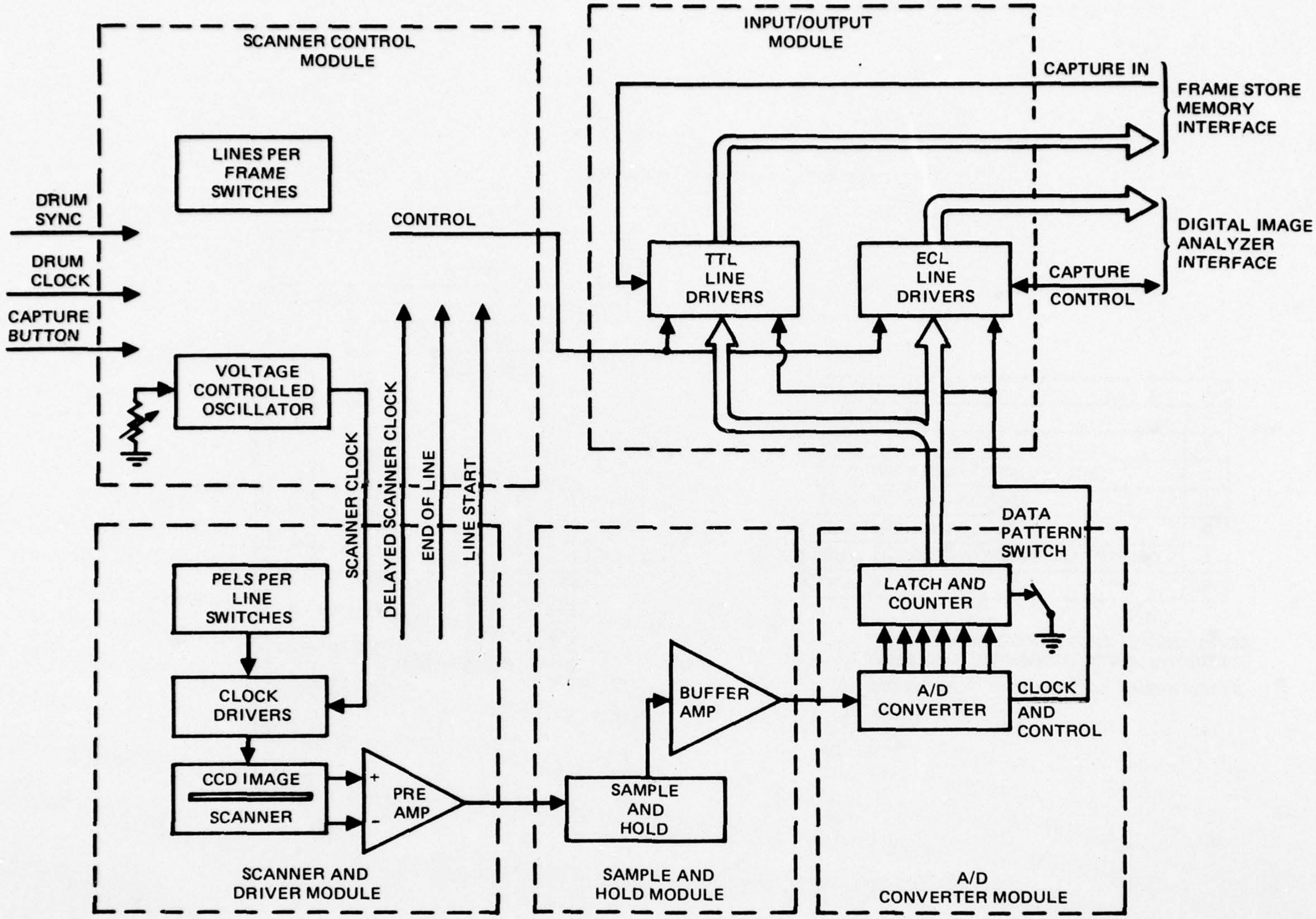
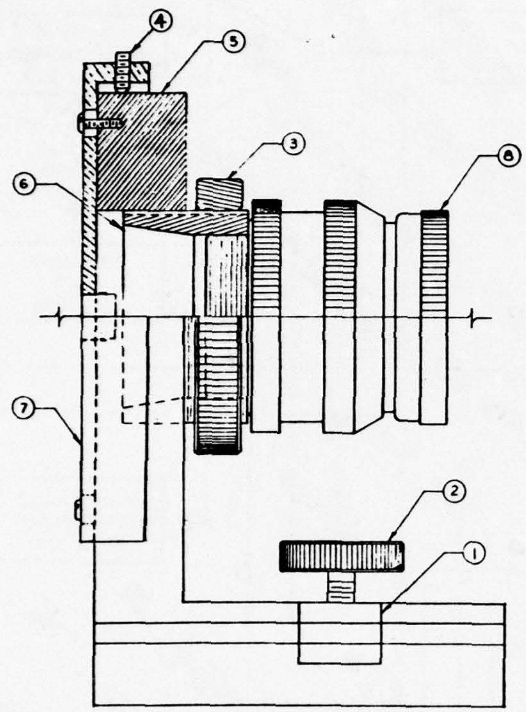


Figure C2. Test bed data flow.



NOTES:

1. SCALE: NONE
2. TOLERANCE: $\pm$.010 EXCEPT WHERE NOTES
3. MATERIAL: ALUMINUM, BLACK ANODIZED, ALL PARTS EXCEPT LOCK SCREW—BRASS

LENS, 55 mm, F/1.4	8
CIRCUIT CARD & SCANNER MTG BOARD	7
FOCUSING RING	6
LENS-SCANNER MOUNT	5
SCANNER MICRO HEIGHT ADJUST	4
JAM NUT	3
LOCK SCREW	2
SLIDE LOCK	1

Figure C3. Lens-scanner assembly.

be adjusted vertically so that the imaged area is exactly normal to the imager. The signals that enter or exit, including power, come from the circuit board enclosure. Data from the CCD image scanner are fed through a type 733 preamplifier to the sample and hold module in the electronic circuit board enclosure.

SAMPLE AND HOLD. The video from the scanner is analog in amplitude and pulse in time. In addition, the actual data pulses are interspersed among clocking pulses. In order to separate the actual video from all the "noise" and to stretch the pulses for later usage, a sample and hold module is utilized. The actual unit used is a Datel systems SHM-UH and is mounted in the circuit board enclosure. The acquisition time is 50 nanoseconds.

A/D CONVERTER MODULE. The analog data coming from the sample and hold module are converted to 6-bit digital data for transmission to the remote processing hardware. The converter used is a Datel Systems ADC-UH6B, which has a conversion rate of 10^7 pels per second. This hardware makes up another card in the circuit board enclosure.

INPUT/OUTPUT MODULE. The output curcuitry of the A/D converter is not adequate for transmitting the high-speed digital data to the remote processing cabinets. National Semiconductor 75114 line drivers are used to transmit the 6-bit digital data.

OPERATION

This test bed was completed and put into operation in the spring of 1975. It was used for the development of the image analyzer and frame store memory hardware continuously until late May 1976, when the power supplies and circuit board enclosure were transferred to the large drum test bed (LDTB). Various aspects of its performance are discussed in the paragraphs that follow.

ILLUMINATION PROFILE. A uniform white test target was put on the scanner drum and the illumination from the Dest Data projector was measured with a Gamma Scientific photometric telescope positioned on the scanner bench. The relative intensity was measured along the axis of the drum and perpendicular to the axis (along the circumference). Tabular results of these tests are given in appendix A (to this appendix). Figures C4 and C5 show the results of the tests. Examination of figure C4 reveals two problems: more fall-off of intensity on one side, which is due to the cold air blowing over that end first; and a lot of ripple in the illumination, which is the result of the filament support wires that are just over 1/2 inch apart. Figure C5 shows the effects of the wires even more dramatically. Figure C6 is a compilation of both the horizontal and vertical photometric scanning data. The uneven cooling could easily be changed by redesign, but elimination of the filament support wires would mean a major program with the lamp manufacturer.

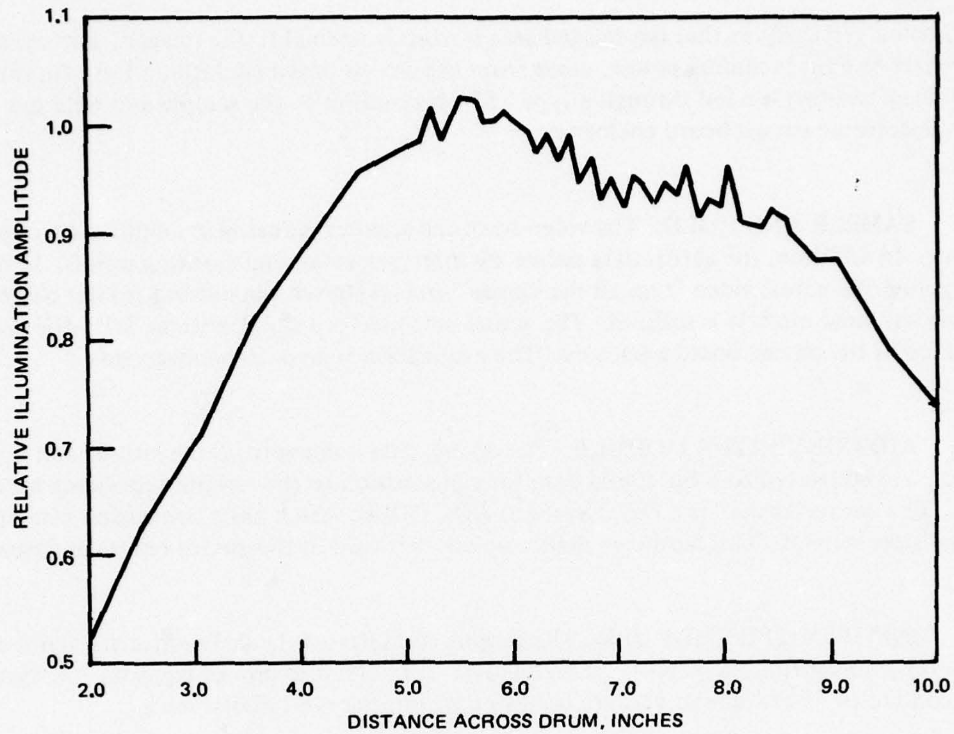


Figure C4. General profile of illumination amplitude vs horizontal position, tungsten source.

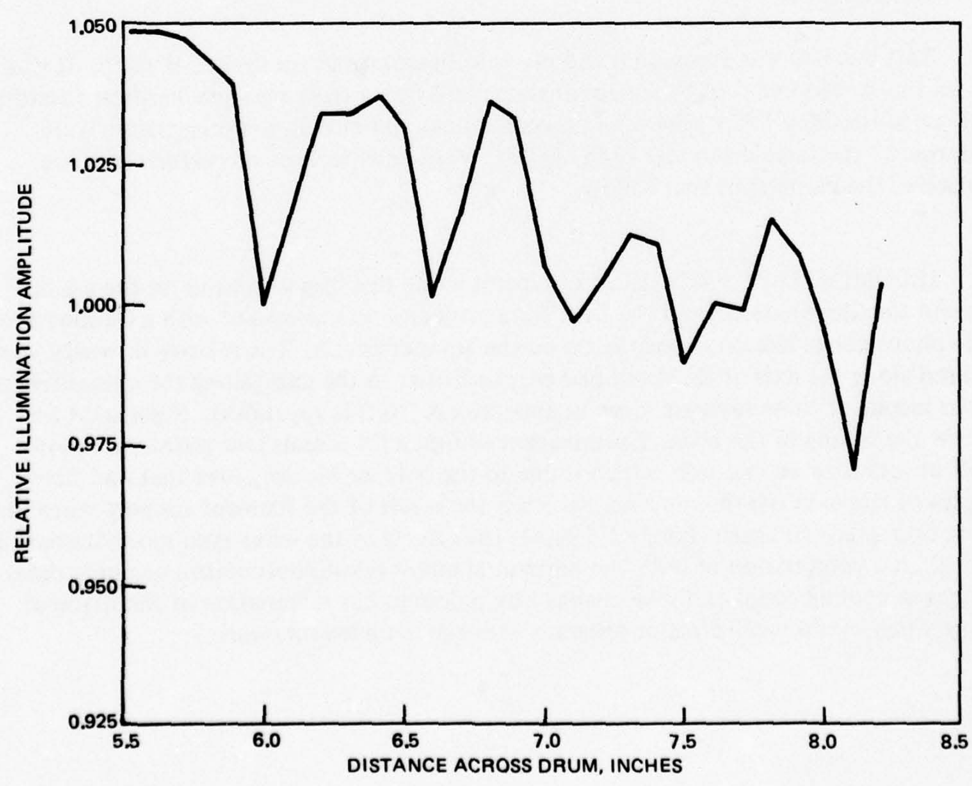


Figure C5. Fine detailed profile of illumination amplitude vs horizontal position, tungsten source.

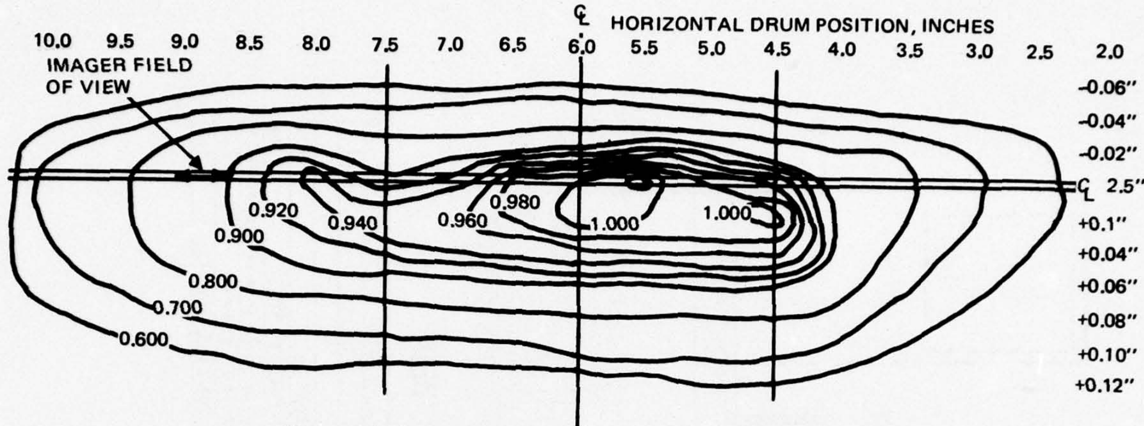


Figure C6. Scanner illumination intensity contour plot.

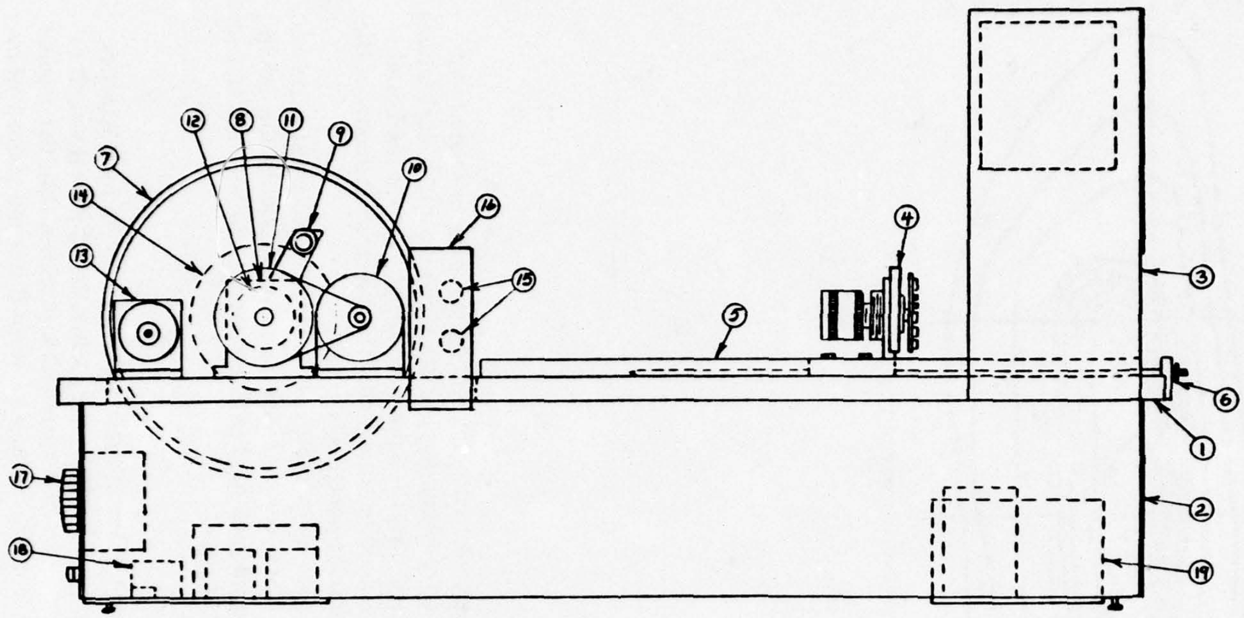
LARGE DRUM TEST BED

PHYSICAL DESCRIPTION

The LDTB (fig C7 and C8) was built to develop and dynamically evaluate more sophisticated imager techniques. The large-circumference drum and shaft encoder features were incorporated in order that advanced tests for equipment being built for the Postal Service by nongovernment contractors could be simulated. The major components of the system are described briefly in the following paragraphs.

Some parts of the SDTB were used on this test and will not be described again except where a modification was made. These parts include the scanner module; the circuit board enclosure, which includes the sample and hold, A/D converter, and line drivers; and the power supplies for the electronic circuitry.

SCANNER BENCH. The bench top for this test bed is 14.5 by 45 by 0.9 inches. The rails used as legs for the bench top are 8 by 43 by 0.5 inches, and the total weight of the three parts is about 80 pounds, making an even more stable platform than the original test bed. This test bed will allow for a working distance between drum and scanner of over 30 inches.



FORTY INCH CIRCUMFERENCE DRUM TEST BED

DRUM SUPPORT BEARING BLOCKS	8	LAMP HOUSING	16		
41 INCH CIRCUMFERENCE DRUM	7	FLUORESCENT LAMPS	15		
SCANNER FINE FOCUS ADJUST	6	SHAFT ENCODER	14		
SCANNER ADJUST GUIDES	5	1/2 RPM MOTOR ASSEMBLY	13	DRUM SHAFT	21
SCANNER ASSEMBLY	4	1 STEP AUX. PULLEY	12	DRUM SUPPORT PLATES	20
CIRCUIT BOARD ENCLOSURE	3	3 STEP PULLEY	11	CARD ENCLOSURE POWER SUPPLIES	19
BENCH SUPPORT RAILS	2	900 RPM MOTOR ASSEMBLY	10	LAMP POWER SUPPLY	18
BENCH TOP	1	JACK SHAFT ASSEMBLY	9	POWER CONTROL PANEL	17

Figure C7. 40-inch-circumference drum test bed.

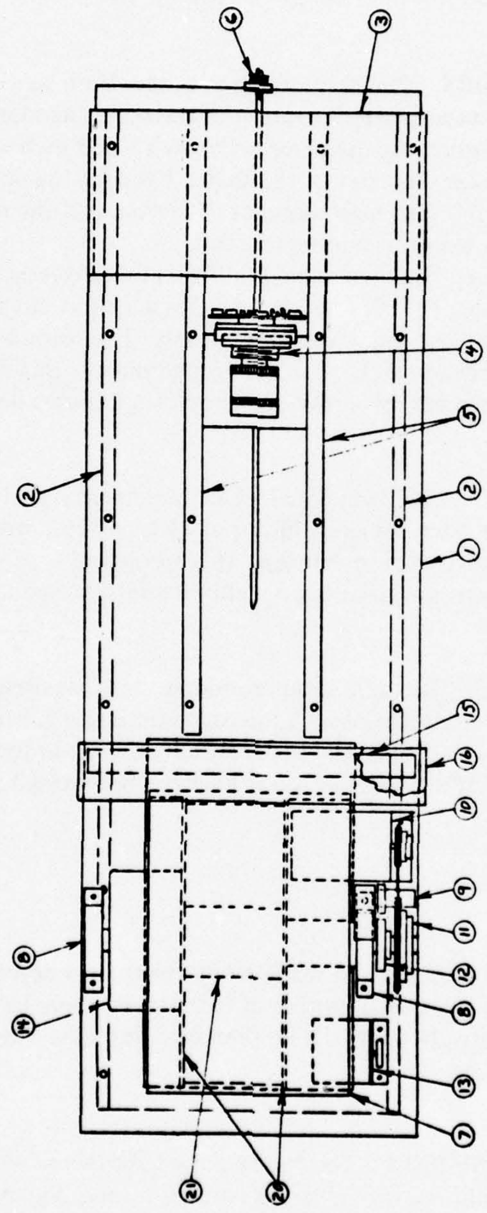


Figure C8. Test bed, top view (refer to fig C7).

ILLUMINATION SOURCE. The illumination source for this test bed is two special high-brightness fluorescent lamps. The initial testing is being done with some 122P99 lamps used in Xerox copiers. Later, F18T8H lamps with a mixture of red, green, and blue phosphors will be installed. They are nominally 33-watt lamps in 15-watt envelopes. For use with the high-speed scanners, the lamps must be operated with either high-frequency ac or dc power. A dc supply is used in this system and is mounted below the drum.

DRUM AND MOTORS. The circumference of the drum was chosen to give exactly 0.005 inch of surface movement per pulse output of the shaft encoder. With 8192 pulses per revolution from the encoder, the diameter becomes 13.038 inches. The drum is hollow except for the 2.5-inch average diameter of the shaft. Even so, the entire drum assembly has a very high moment of inertia. The high moment of inertial and the usage of precision ground bearings should yield a very smooth running test bed.

Two motors have been installed. One is a 900-rpm hysteresis synchronous motor that can drive the drum at 20, 15, 10, 8, 6, or 4 pps by selection of various pulley combinations. As before, O-ring rubber is being used for belting. The second motor is 1/2-rpm hysteresis synchronous gearhead clock motor. Through pulleys this motor will drive the drum at the rate of 6 minutes per revolution, or about 1.6 minutes per page.

SHAFT ENCODER. A Baldwin 5V675HAZ incremental shaft encoder was mounted on the drum shaft. This encoder has a resolution of 213, or 8192, pulses per revolution. It also puts out a sync pulse once each revolution. It is an optical type with very good precision. Detailed specifications are given in appendix B (to this appendix).

IMAGER MODULE. The same scanner module that was used on the SDTB is used on this test bed with some modifications. A micropositioning mechanism was added for fine focus adjust when the lens being used does not have a built-in focusing ring. The other modification made was the addition of a "quick change" mounting technique for the scanner and circuit board.

OPERATION

This test bed was completed and made ready for system development work during the last week of May 1976. As of the writing of this report, there have been very few new data developed based exclusively on its usage; therefore, the following paragraphs will discuss primarily planned testing.

ILLUMINATION PROFILE. The Xerox copy lamps were tested for uniformity in March 1976 prior to ordering the special lamps from Sylvania. Figure C9 shows the relative intensity profile for one of the Xerox lamps. The maximum intensity change of about 7% over the center 8.5 inches is decidedly better than the 30% drop-off experienced with the

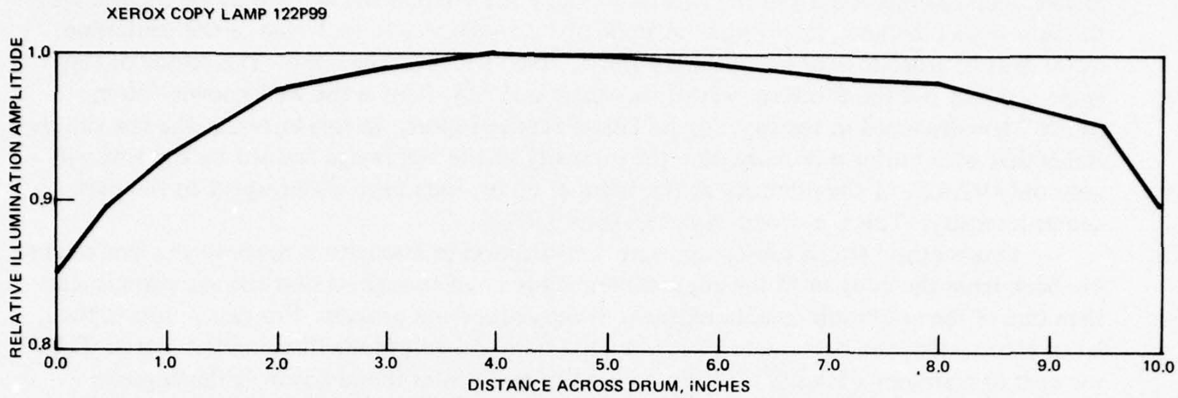


Figure C9. General profile of illumination amplitude vs horizontal position, fluorescent source.

Dest Data projector at each end of the 8.5-inch span. Furthermore, the intensity transition from one end to the other is perfectly smooth (one lamp tested had a phosphor blemish, but this is a quality control matter as opposed to a technique problem), whereas the halogen lamp yielded about 3% intensity variation for each filament support wire.

PLANNED ILLUMINATION CORRECTION. The initial attempts at illumination correction will be made in software programs using the frame store memory and memory controller. It is anticipated that this will be a slow and laborious process, since it may be necessary to use the magnetic tape deck for retrieval and storage of uncompensated and compensated images. A hardware module capable of real-time operation (21 megapels per second) has been designed but not fabricated for future compensation studies.

The problem of nonuniformity of illumination with the single-filament quartz iodide lamp has been discussed in a previous section. The promise of a much more uniform illumination using the fluorescent tube envelopes has also been discussed. There are, however, two remaining sources of nonuniformity in the optical-to-electrical conversion process. One of these sources is the nonuniformity of the optical-to-electrical conversion and the charge transfer efficiency of the imaging device itself. This will be discussed in a later section. Another contributor to optical nonuniformity is related to the quality and positioning of the lens assembly itself.

Appendix C (to this appendix) includes the calculation for the employment of a 55-mm photographic lens. This lens is the f3.5 Micro Auto Nikkor P55. This lens is one of the sharpest lenses available in 35-mm photography with a very high center-to-edge resolving power. It is equally applicable for its extreme flatness of field and high image contrast. Lenses having all the foregoing attributes will be required in order to provide the image fidelity stated in the Postal Service goals.

The calculations in appendix C show that if a 55-mm lens is used in conjunction with 8.5-inch copy material and a Fairchild CCD121 line imager having an optical aperture of 0.890 inches, then the distance from the lens to the copy material on the drum is 22.85 inches. For this lens-object distance there exists an angle of 10.54 degrees to each side of the centerline of the lens in order to accommodate the full 8.5-inch width of the copy. The cosine of this angle is 0.983 and the fourth power of this angle is 0.934. This is the well known "cosine fourth" law discussed in the first annual Postal Service report. In this instance, the law simply states that with uniform illumination, the intensity of the real image formed by the lens will have only 93.42% of the intensity at the edges of an 8½-inch page with respect to the page center intensity. This is a droop of 6.58% (or ±3.29%).

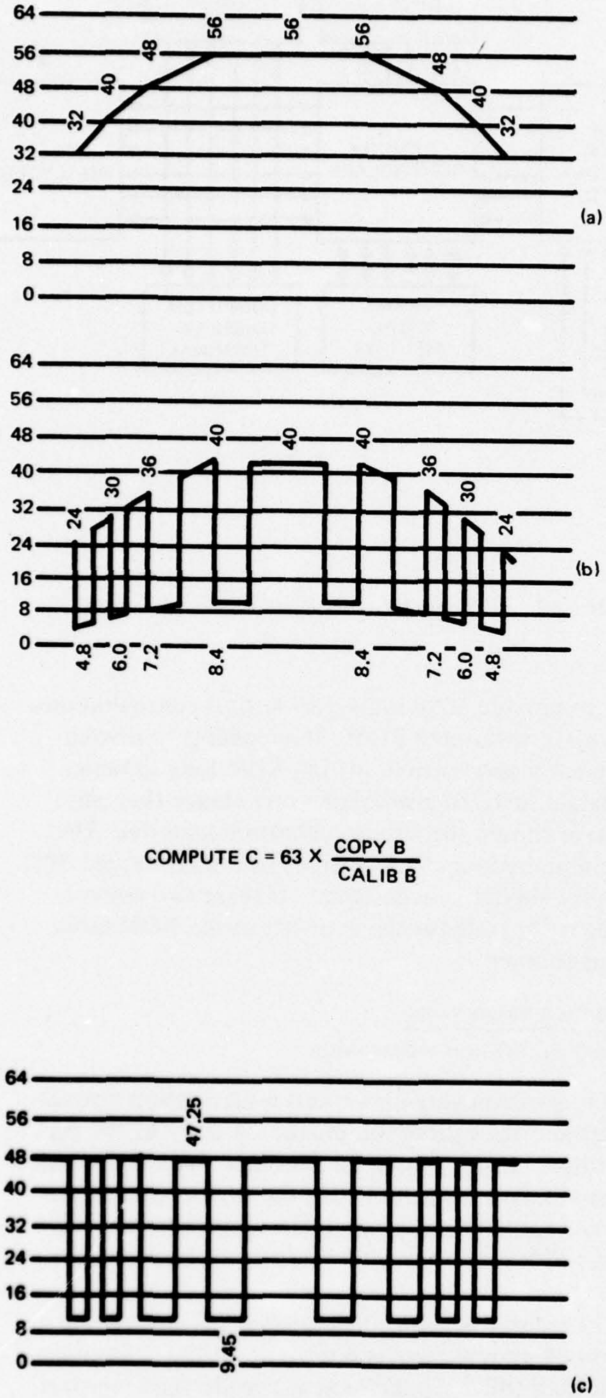
One method which can circumvent this variation in intensity is to move the lens assembly back from the copy until the angle subtended is small enough so that the variation is less than one of the amplitude quanta required in the acquisition process. For this purpose, then, let us assume that the data are to be acquired in 64 equal-amplitude illumination levels. Then we wish to maintain a fidelity of at least 63/64 of this center illumination at the edges in order to preclude the loss of data at these points. The fraction, then, of 63/64, or 0.984, must equal the fourth root of this number and solving for the cosine gives an angle of 5.08 degrees. Given a copy width of ±4.25 inches and an angle subtended of 5.08 degrees, it can be shown that the lens assembly must be 47.8 inches away from the copy.

The above optical calculation only satisfies the "cosine fourth" law for an evenness of illumination to better than plus or minus 1/2 lsb brightness amplitude. Yet all the other static or repetitive errors that might have occurred due to vignetting of the lens, unevenness of original illumination at the copy, and unevenness of optical-to-electrical conversion and shift-out of the image data still remain. Secondly, it is now necessary to procure a high-quality, long-focus lens having a flat field and aplanatic characteristics which are suitable for line and area tracking imaging.

An investigation has been made into the alternate methods of providing corrections for these redundant errors in the image acquisition system. The simplest strategy devised thus far can be seen in figure C10. This method requires that a calibration scan be taken with a uniform target of the whitest material available. For our application we have selected Eastman white reflectance paint which is a barium sulfate ($BaSO_4$) mixed with a binder material which can be sprayed onto a rigid bar which in turn can be bolted to the test drum. The acquired calibration curve may have an appearance similar to that shown in figure C10a. The values of pel brightness amplitude as shown in this profile are digitized to 6 binary bits as the calibration curve is obtained. As the profile is obtained the 6-bit words are stored in a suitable storage register as shown in figure C11.

Analog input data are presented through the preamplifier and an A/D converter as in conventional image acquisition. A branch of the digitized data outputs is fed to the pseudorandom shift register which is in fact a static random access memory (RAM). In order to accommodate at least 1700-pel width at 6 bits per pel, it is necessary to provide a static RAM with at least this capability. In the figure, a 2048-word by 6-bit shift register is shown. For our design goal of 84 megapels per second from four or more ports, it is necessary for the data acquisition and read-out rates to be at 21 megapels per second.

A read only memory (ROM) table of 2048 words by 6 bits is placed in the data path in such a way that 6 bits from the analog-to-digital converter and 6 bits from the output of the static (RAM) are used as addressed inputs.



STEP 1. RUN CALIBRATION CURVE WITH WHITEST MATERIAL. STORE SEQUENTIAL VALUES OF REFLECTIVE BRIGHTNESS.

STEP 2. RUN ROUTINE COPY DATA. ACQUIRE SEQUENTIAL VALUES OF REFLECTIVE BRIGHTNESS.

$$\text{COMPUTE } C = 63 \times \frac{\text{COPY B}}{\text{CALIB B}}$$

STEP 3. DIVIDE THE COPY BRIGHTNESS VALUES AS RECEIVED BY THE STORED CALIBRATION VALUES. MULTIPLY BY CONSTANT = 63 AND PIPELINE OUTPUT TO PRESTORAGE PROCESSOR OR FRAME STORE MEMORY.

STEP 4. STORE, PROCESS, ANALYZE, AND/OR DISPLAY CORRECTED RESULTS.

Figure C10. Illumination correction.

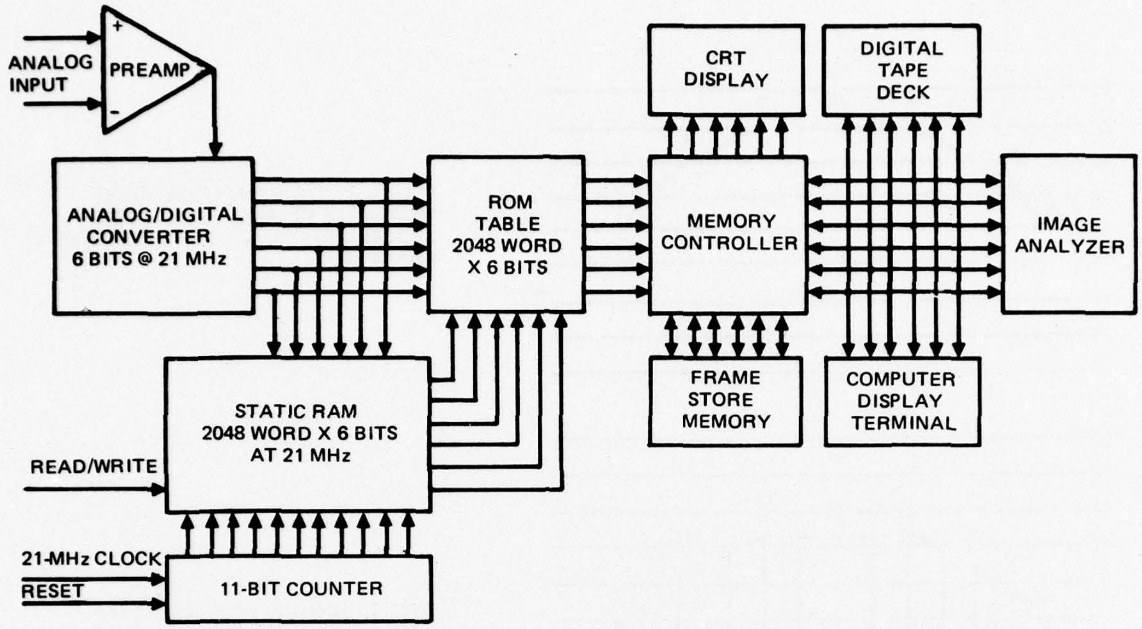


Figure C11. Acquisition system, block diagram including illumination correction.

With 12 inputs it could be possible to provide 4096 individual output configurations of data which would be programmed and stored within the ROM. It is possible to invoke two simple design assumptions which will greatly save capacity of the ROM lookup table. The first is to assume that the calibration target material gives higher reflectance than any USPS copy material. If this is not so, we have chosen the wrong calibration material. The second assumption is that the droop in the illumination characteristics will never exceed 50%. If this is not true, then the illumination source should be redesigned. If these two assumptions are accepted, it is possible to write the truth table for the contents of the ROM table. Contents of the ROM table are calculated as follows:

$$\text{Compensated output value, } C = 63 \times \frac{\text{incoming video value}}{\text{stored calibration video value.}}$$

In effect, the ROM is programmed to perform very-high-speed 6-bit division normalization of values as received from the imager and the calibration profile. A copy of the partially filled-in ROM truth table is shown in figure C12. Notice the fact that two rules which were invoked at the beginning of the discussion have truncated both the top portion of the truth table and 50% of the values running horizontally across the table. It is therefore relatively easy to calculate the program for a set of ROMs to provide this very-high-speed calibration correction function.

There exist very few high-speed shift register devices which have speed and capacity parameters commensurate with this logic problem of storage and retrieval of the calibration sample. There are, however, a few RAM devices which can be used as pseudo shift registers at these speeds.

CALIBRATION VALUES

UNKNOWN VALUES	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
63	63																															
62	62	63.0																														
61	61	62.0	63																													
60	60	61.0		63																												
59	59	60.0			63																											
58	58	58.9				63																										
57	57	57.9					63																									
56	56	56.9						63																								
55	55	55.9						67.9	63																							
54	54	54.9						60.8		63																						
53	53	53.8						59.6			63																					
52	52	52.8						58.5				63																				
51	51	51.8						57.4					63																			
50	50	50.8						56.2						63																		
49	49	49.8						55.1							63																	
48	48	48.8						54.0								63																
47	47	47.8						52.9									63															
46	46	46.7						51.8										63														
45	45	45.7						50.6											63													
44	44	44.7						49.5												63												
43	43	43.7						48.4													63											
42	42	42.7						47.2														63										
41	41	41.7						46.1															63									
40	40	40.6						45.0																63								
39	39	39.6																							63							
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13	13	13.2																														
12	12	12.2																														
11	11	11.2																														
10	10	10.2						11.																								
9	9	9.2																														
8	8	8.1																														
7	7	7.1																														
6	6	6.1																														
5	5	5.1																														
4	4	4.1																														
3	3	3.0																														
2	2	2.0																														
1	1	1.0																														
0	0	0.0						00.0																								

ALL VALUES ABOVE 63 ARE INVALID

$$C = 63 \times \frac{\text{UNKNOWN VALUE}}{\text{CALIBRATION VALUE}}$$

Figure C12. Calibration of ROM table values.

Figures C13 and C14 show a logic block diagram and the timing wave forms of a variable-length, high-speed pseudo shift register. This approach uses 1024-by-1 RAM devices for the memory. In this case, Signetics devices type N82S11 has been selected as the storage device for this application. Since this drawing was made, Signetics and a second source, Teledyne, also now provide an even higher-speed device, the N82S111.

Although these are very-high-speed devices, the read/write cycle time is such that demultiplexing is necessary in order to reduce the read-modify-write requirement by a factor of two.

The complete operation, then, for using the calibrate (illumination) strategy would be as follows:

1. The brightness profile for the calibration strip is stored in the static RAM at 6 bits per pel digitized resolution. No further data need be written into this memory until such time as recalibration is required.

2. As routine sheets of USPS copy are fed through the system, values of the digitized image data along with corresponding values of the stored calibration curve data are presented pel by pel to the ROM address inputs.

3. Using the address data above, the ROM provides a 6-bit compensated output value, which is used for further prestorage processing and buffer storage.

It should be pointed out there that there are also other applications for a module which will hold individual digitized lines of scanned data. The illumination calibration requirement is only one of several. Two or more of such lines of data probably will be required if two-dimensional edge enhancement techniques are ever to be studied or accommodated in real time. A third application for retaining past history samples of scanned data is for two-dimensional data compression techniques. One such strategy may call for a meandering run length technique, which is expected to increase the length of runs appreciably. Another possible application for compression is in the use of differential pulse code modulation (DPCM) techniques from scan line to scan line. There probably will be high correlation in the direction of copy motion from line to line as sample pels of typed or handwritten characters, map data, or to some extent continuous tone pictures are scanned. A block diagram (fig C15) shows how two delay line modules would be employed to provide concurrent data from a presently scanned line plus the two previous lines.

SCANNERS TO BE TESTED

During early operation of the SDTB, the test bed and the Fairchild CCD110 scanner mounted on it were essentially assumed to be a test signal generator and the remote equipment was the items under development and test. The development of the remote equipment has progressed to the point at which it now serves as a test facility for evaluating scanners mounted on the LDTB. The scanners to be tested and/or operated include:

1. Fairchild CCD121, a 1728-element linear scanner
2. Fairchild CCD110, a 256-element linear scanner
3. RCA TC1155 camera with a "surface channel" area scanner installed
4. The same RCA TC1155 camera with a "special" area scanner installed

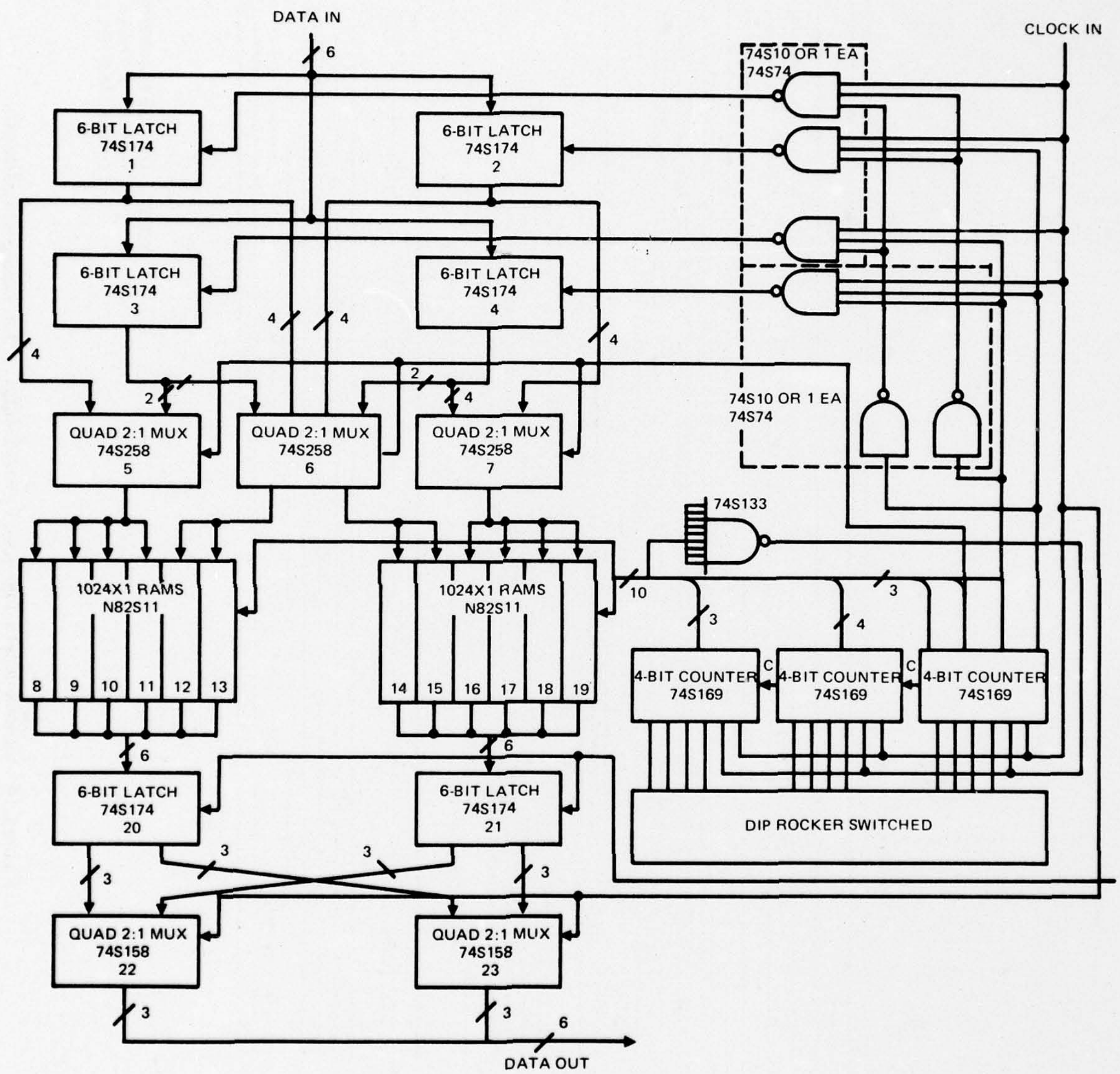
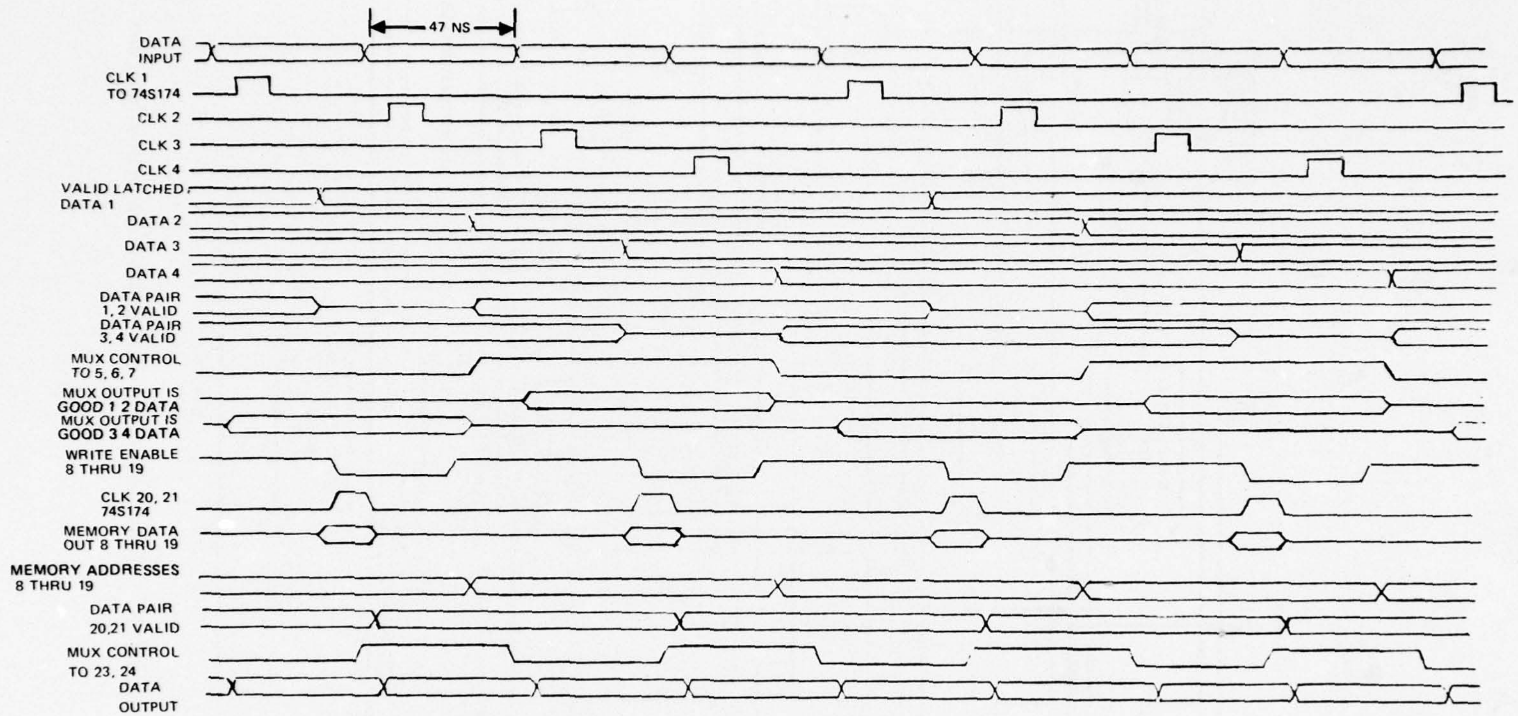


Figure C13. Variable-length, high-speed pseudo shift register, logic block diagram.



NOTE: DEVICE NUMBERS REFERENCED REFER TO THOSE ON BLOCK DIAGRAM (*FIG C13*)

Figure C14. Variable-length, high-speed pseudo shift register, timing wave diagram.

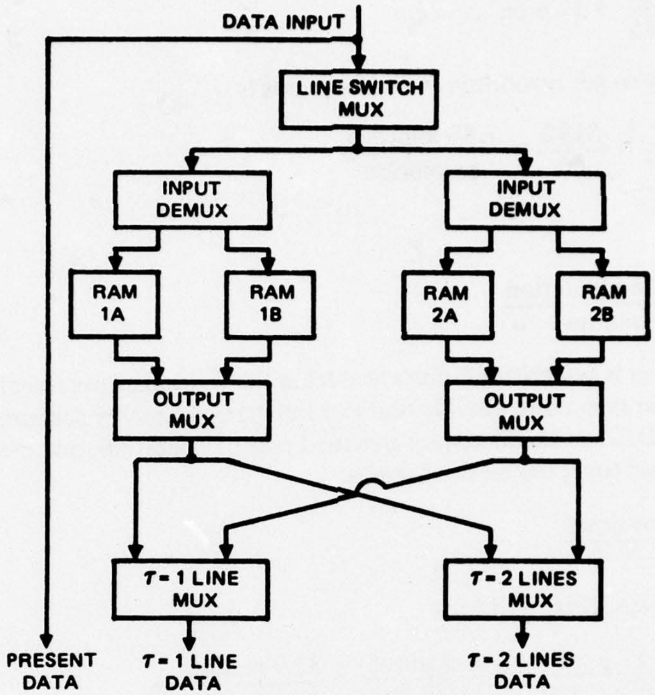


Figure C15. Scan sample delay lines, block diagram.

The first three are discussed briefly below. The fourth is described at more length in a separate section.

FAIRCHILD CCD121. The CCD121 (1728 pels) will be used (after all circuitry is debugged) to generate full-page, high-quality images for storage on magnetic tape. The images stored on the magnetic tape can then be used as test signals for advanced development of enhancement and compression techniques. Information is being formatted on the tapes so that in the future full-page printouts can be obtained from the Image Processing Institute at USC, Perkin Elmer Company in Pasadena, or RCA in Camden, NJ. The device and its driver electronics are being debugged at this time.

For the acquisition of data using the Fairchild CCD121 and recording the images on the Kennedy tape deck, theLDTB scanning drum must be rotated very slowly. The calculations for the line acquisition rate are as follows:

Time to transfer data to tape,	$T_1 = 24.1$ ms
Time for tape record gap, burst and stop	$T_2 = 24.8$ ms
Minimum time per acquired line	$T_3 = T_1 + T_2 = 48.9$ ms.

Since there is about ±15% variation in the uniformity of time periods between the 0.005-inch pulses (probably due to stiction) at these low speeds, the nomonal line acquisition rate must be

$$T_4 = \frac{T_3}{0.85} = 57.6 \text{ ms} \ .$$

Then the total time per revolution for 8192 pulses is

$$T_5 = T_4 \times \frac{8192}{60} = \frac{7.80 \text{ minutes}}{\text{revolution}}$$

or

$$\frac{1}{T} = \frac{0.128 \text{ revolution}}{\text{minute}}$$

Since there is bountiful illumination from the Sylvania fluorescent lamps, it is desirable to minimize smear and provide uniform integration time by scanning the data from the Fairchild CCD121 at its maximum specified rate of operation, one megapel per second. Including overhead time, the readout rate is

$$R_1 = \frac{1 \text{ readout}}{1.76 \text{ ms}}$$

Then at these speeds, there will be

$$N_1 = \frac{57.6 \text{ ms}}{0.005 \text{ in scan}} \times \frac{1 \text{ readout}}{1.76 \text{ ms}} = \frac{32.7 \text{ readouts}}{0.005 \text{ in scan}} \ .$$

If the system is programmed to accept the first full scan line after each 0.005-inch encoder pulse, the position accuracy will be

$$S_1 = 0.005 \text{ inches} \pm \frac{0.005 \text{ inches}}{32.7 \text{ readouts}} = 0.005 \pm 0.00015 \text{ inches},$$

which is ±3%.

The CCD121 failed to operate properly when it was first installed in the test bed. Although the device is mounted in a larger dual in-line package (DIP) having 24 pins on 100-by 660-mil centers rather than the 18 pins which the CCD110 has on 100-by-300-mil centers, the number of signals required is the same for both. Also, the specified waveforms and amplitudes are generally identical for both devices. An adapter socket was made to accommodate the CCD121 with proper pin assignments, but initial operation was quite poor. No values of readjusted biases or clock amplitudes cleared the problem. Mr Joe Rothstein of Fairchild, Palo Alto, was contacted. From our description of the symptoms and the fact that the device is a new production version, he predicted that the device was charge injecting due to clock swings having voltage excursions more negative than the substrate and activating protection diodes. We clamped the clocks with 1N914 diodes to prevent negative excursions and the scanner began to operate properly.

An attempt was made to improve the video response in the circuit by dc coupling the video amplifier chain. This worked exceedingly well unless the light amplitude around the first three or four pels was modulated. A variation in light amplitude at this end of the device caused the dc level of the entire device to change markedly. Dimming the light on the first three pels caused an increase in the entire line response. A sensitive, high-impedance scope was connected to the video output of the chip. No output dc change was noted with the illumination change. The scope was moved to the chip's compensation output and an appreciable change in dc voltage was noted with a variation in impinging light.

We again contacted Fairchild, Palo Alto, and talked to Mr Howard Murphy. He mentioned that the devices had "peripheral response," but that this was not the same symptom. He said he would try the same test on their setup and call us back. He called back the next day and said their units did not respond the same way. Both NELC units reacted identically when tested here.

A decision was reached to revert to ac coupling with a gated clamp. The present circuit contains ac coupling into the type 733 amplifier and on the differential output. After the second pair of capacitors, both signals are clamped between pel output pulses. The circuit and the device are now performing very well, but neither we nor Fairchild understand the nature of the light-sensitive offset of the compensation amplifier. When time permits, this will be investigated. The entire LDTB, including the imaging path for full 8½-inch copy, is now ready to send data to the frame store memory at rates up to one megapel per second. At these speeds the response is such that an aperture of f8.0 is adequate with the present light source.

FAIRCHILD CCD110. The CCD110 (256 pels) scanner will be used primarily for purposes of demonstration of the entire system as the situations demand. This is the same device that was used with the SDTB.

RCA TC1155 CAMERA IN TRACKING MODE. The RCA TC115 camera as originally built is a standard 525-line, closed-circuit TV camera using the RCA SID51232 surface channel CCD device. The expected performance of the camera in this configuration is discussed later in this report. The camera has been returned to RCA for modifications that would allow it to be operated in limited image tracking mode. When the camera is returned (with the surface channel device still in place), the camera will be mounted on the LDTB for operating in the tracking mode. After such time as it takes to debug the tracking mode operations and performance data have been collected, the camera will be returned to RCA again for installation of a special device. This device will be loaned to the program for a period of 1–2 months; during that time the camera will again be mounted on the LDTB and operated in the tracking mode for comparative tests and data collection.

RCA TC1155 ALL SOLID-STATE CAMERA–AREA IMAGING

THEORY OF OPERATION

The RCA TC1155 All Solid-State Camera employs the use of the SID51232 Area Imaging Device. The operation of this device for acquiring two-dimensional images is shown in figure C16. The device itself is a single silicon bar containing 320 vertical surface channel CCD arrays spaced on 1.2-mil centers. The upper 256 and the lower 256 three-phase clock sections have separate clock control lines so that data can be manipulated separately in the upper half and the lower half or, if desired, can be manipulated in synchronism from one half to the other.

At the bottom of the array there exists one high-speed horizontal CCD surface channel shift register which allows the contents of the vertical shift registers to be swept from the

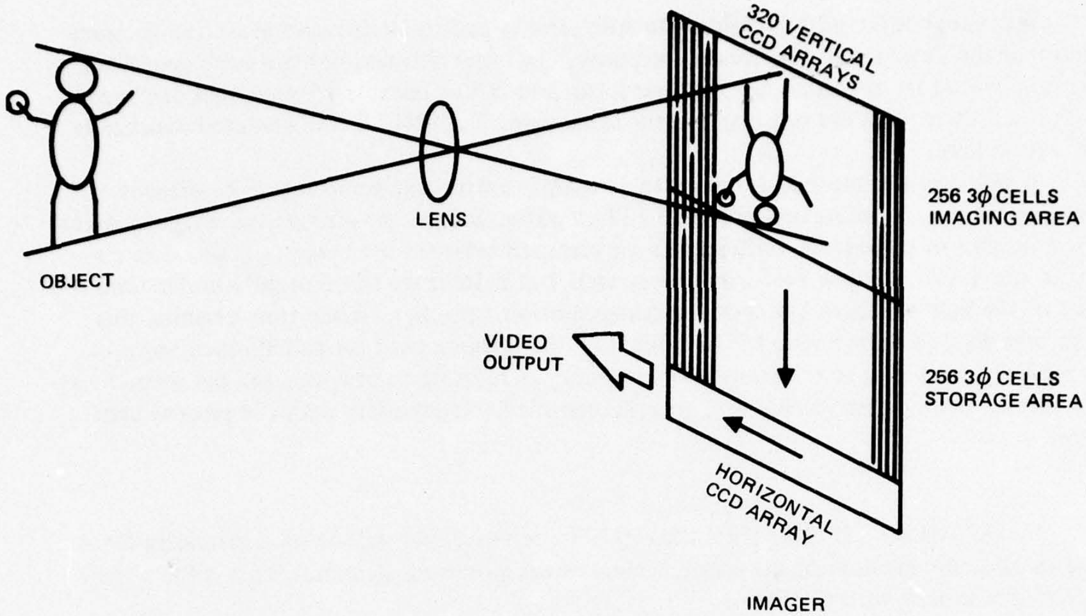


Figure C16. RCA TC1155 camera imaging system using SID51232.

bottom of the array as 320 pel signals are deposited onto the horizontal array. The output rate of the horizontal register is at least 6.2 megapels per second. The specified vertical transfer rate of the vertical shift register is 280 kilopels per second.

In the TC1155 camera, the lower half of the device is not used for optical image acquisition. Alternatively it is used for the temporary storage of the previous field of data, which is shifted slowly out to the horizontal shift register as rapidly as the video can be generated.

In operation the optical half of the device (320-by-256 pels) remains unclocked for a period of one field time (approximately 16 milliseconds). At the end of this period, during vertical retrace, the clocks for the optical half of the device and the storage half of the device are operated together rapidly. This quickly shifts the electrons gathered in the photosites from the optical half of the device down into the storage half. At this time the clock leads for the upper (optical) half of the device are again disconnected and integration of photoelectrons begins for the alternate field of the frame. The clock leads for the lower storage device are slowed down to about 15.75 kilohertz per three-phase cycle. At this speed, data are fed into and shifted out of the high-speed horizontal shift register at a line and video data rate which is compatible with commercial television.

DIFFERENCES FROM GENERAL ELECTRIC AND FAIRCHILD

The operation of the TC1155 camera is different from operation of GE and Fairchild cameras in some ways. The GE camera employs a charge injection device (CID) which does not shift the video information at all in obtaining an optical image. Electrical signals on

electrodes of row and column pel pairs are manipulated to cause individual data from individual photosites to be fired into the substrate at a spatial rate compatible with commercial television.

The Fairchild area arrays do not use the photosites themselves as the CCD shift registers. Fairchild accumulates data in photosites and then transfers the data alternatively from odd and even field into vertical buried layer CCD channels which are metal masked to prevent optical sensitivity within the CCD array itself. In this manner it is not necessary to provide a separate area of the chip for storage since the storage for each half frame is accommodated within the optically protected vertical CCD channels. Also, it is not necessary to shift the image information at high speeds to the horizontal output shift register. A rate of 15.75 kilopels per second is just adequate to allow the device to operate compatibly with conventional television line and frame rates. The Fairchild area device has a buried layer horizontal output CCD array. The fact that all CCDs on the Fairchild device are in buried layer technology greatly improves the charge transfer efficiency and contrast dynamic range as compared to an RCA surface channel device.

BENCH TEST CHARACTERIZATION OBSERVATIONS

INTRODUCTION

The model TC1155 "Solid-State Imager" Camera was exercised extensively with the aid of a Gamma Scientific Model 125 Microprojector, Bausch and Lomb High-Intensity Grating Monochromator, Conrac 9-inch TV monitor, Tektronix 465 scope, Polaroid C5 Close-Up Camera, various photometric accessories, test targets, and optical filters. In general, the exercises were for the purpose of gaining operational familiarity and qualitative performance data. The following paragraphs describe various tests, results, and observations about the CCD camera performance. The Polaroid camera was used to record the CCD performance as revealed by the TV monitor and corresponding oscilloscope waveforms. Figure C17 shows most of the equipment used in characterizing the performance of the RCA CCD camera. The camera without a lens is shown mounted on the micro-projector.

RESOLUTION

The first testing of the CCD camera involved the use of the microprojector and various high-contrast test slides including the Air Force Three Bar Test Charts. Figures C18a, b, and c illustrate the general performance of the camera. The problem these photographs illustrate is poorer resolution and contrast in the vertical direction as compared to the horizontal, particularly in figures C18 b and c. This characteristic is the result of relatively poor transfer efficiency in the imager. This problem will be demonstrated in more detail with other signals and photographs.

Examination of the TV monitor with the AF Test Chart in the projector revealed ghost images in the horizontal plane. This problem did not show up well in the first photographs so a different test was used. A slit of light 3-by-100 mils was projected onto the imager with a reduction of 1.8:1. The line was positioned vertically and horizontally. The results are shown in figures C19a and b, respectively. Figure 19a clearly shows the ghost images and figure 20a shows the electrical signal causing the ghost. The reason for the

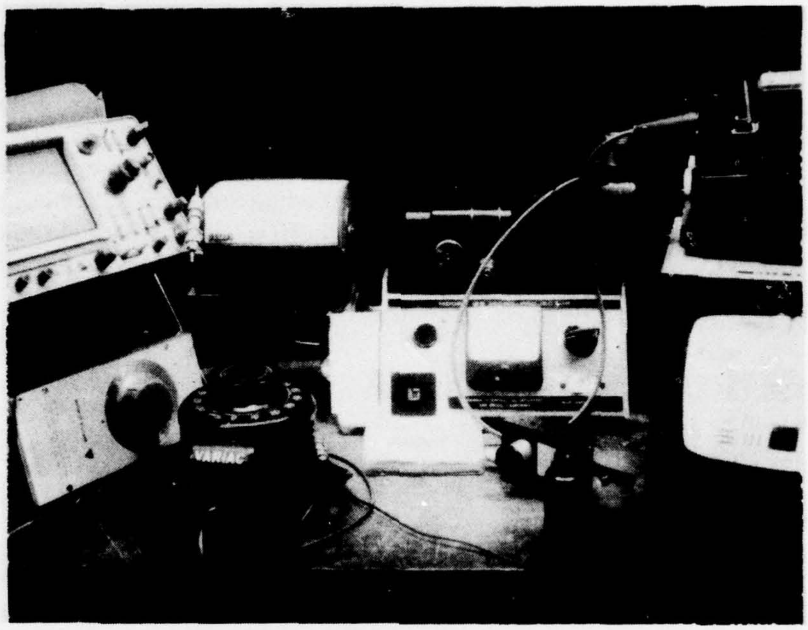


Figure C17. RCA CCD camera and equipment used in its characterization.

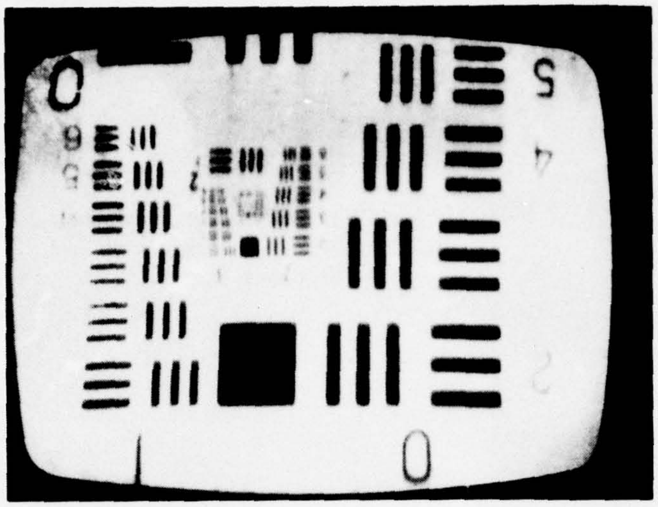


Figure C18a. Air Force Three Bar Test Chart as reproduced by the RCA CCD camera on a TV monitor.

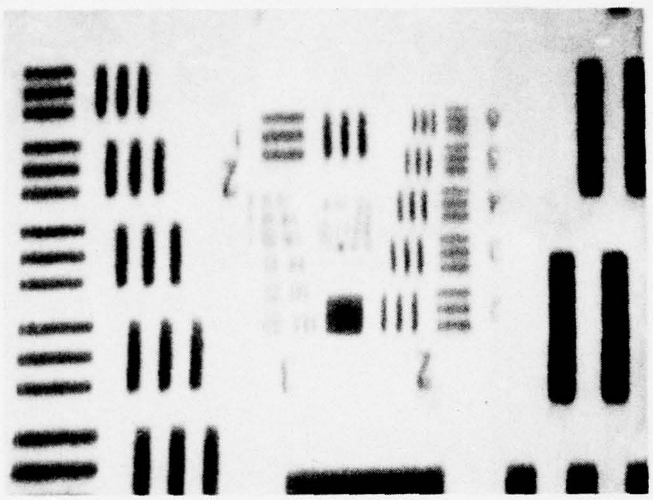


Figure C18b. Center portion of C18a enlarged to better show the difference in horizontal and vertical resolution.

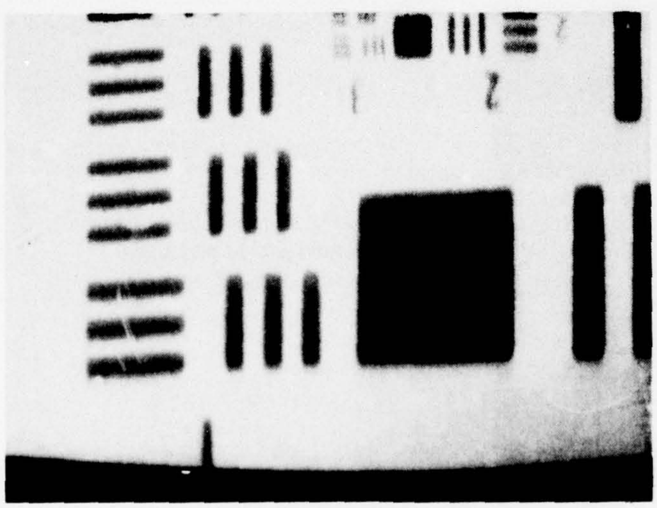


Figure C18c. Lower left portion of C18a enlarged to show variation in resolution.

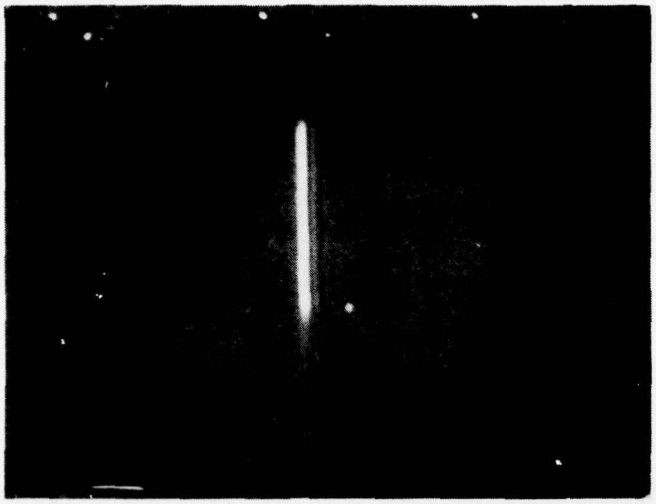


Figure C19a. CCD camera reproduction of a 1.7-by-55-mil slit of light positioned vertically. Note ghost images.

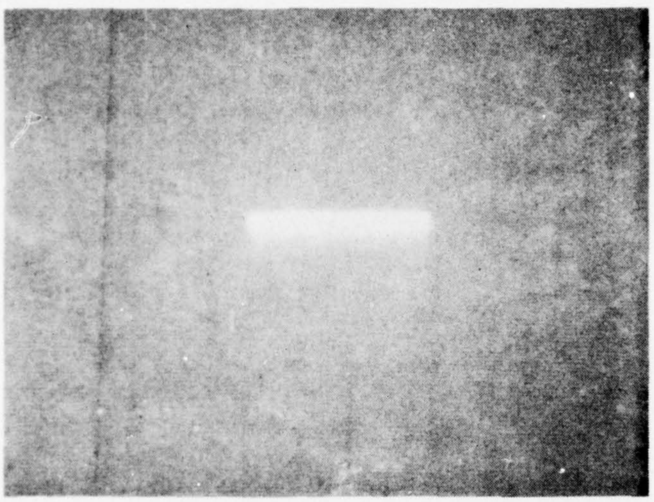


Figure C19b. The same slit of light positioned horizontally.

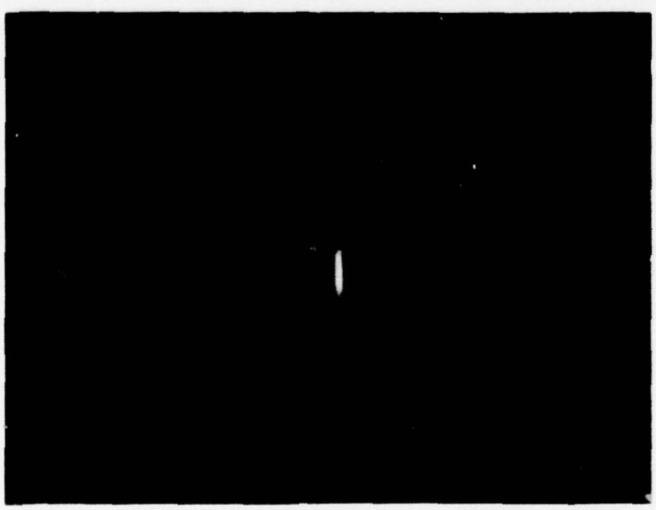


Figure C21a. Reproduction of a 0.4-by-14-mil light slit positioned vertically and centered on a pel.

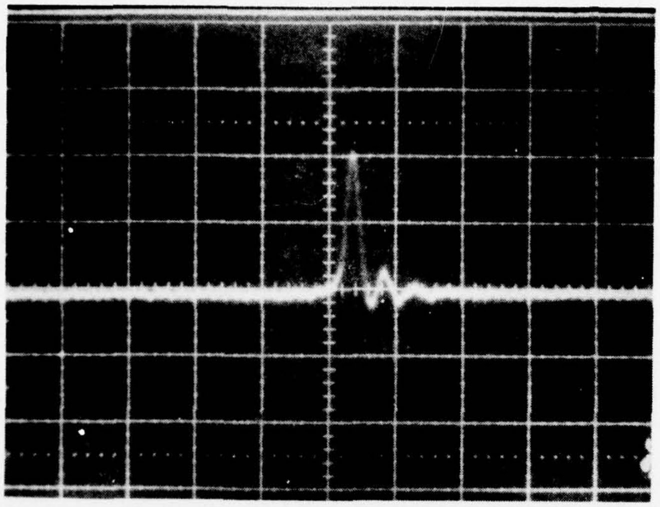


Figure C20a. The video signal on one horizontal line that produces the TV image of C19a.

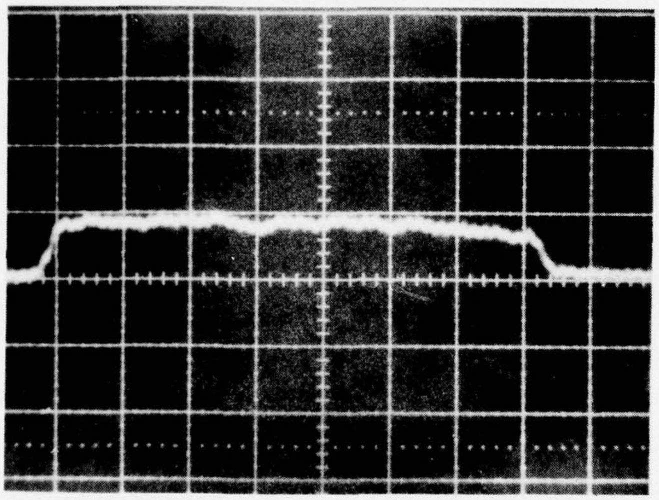


Figure C20b. Video signal for C19b.

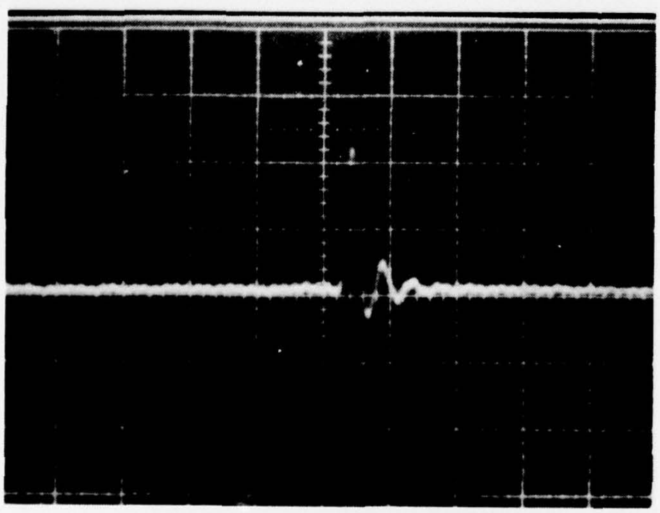


Figure C22a. Video signal for C21a.

ringing is the L-C filters used in the camera circuitry to filter out all the clock noise of the digital circuitry. It probably is not practical to eliminate the problem with better filters and still maintain single-pel resolution. When the camera is used for continuous tone images, this would not be a serious problem, but for reading high-contrast printed material it would be serious. The solution for this application is the "sample and hold" technique.

Figure C19b shows again the poor resolution in the vertical direction, and the comet-like tail below the line is the result of the poor transfer ratio. The limited dynamic range of the photographs makes them a poor comparison device, but comparing the waveform amplitudes in figures C20 a and b reveals a difference of more than 2:1 even though the light intensity was maintained constant.

The 1.8:1 reduction of the 3-by-100-mil light slit gives a light slit at the CCD imager of 1.67 mils, which is almost 1.4 pels (each pel is 1.2-by-1.2 mils). The light slit reduction ratio was reduced to 7.2:1 to give a light slit at the imager of about 0.4 mil or 0.35 pel. Figures 21a, b, c, and d show the results of this test. As before, the light amplitude was held constant. The most interesting point about this test is seen by comparing the pulse width in photographs 20a and 22a—the difference is very minimal. Figures 21d and 22d show the results of positioning the light slit directly over the junction of adjacent pels. Again, the resulting pulse width is not much different. The conclusion to be drawn from this is that the L-C filters used to smooth out the video signal are not necessarily the best choice for single-pel resolution.

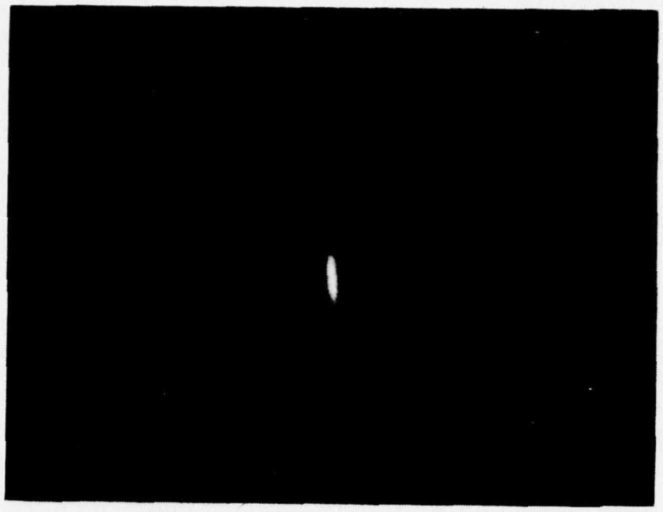


Figure C21b. Light slit positioned at 45 degrees.

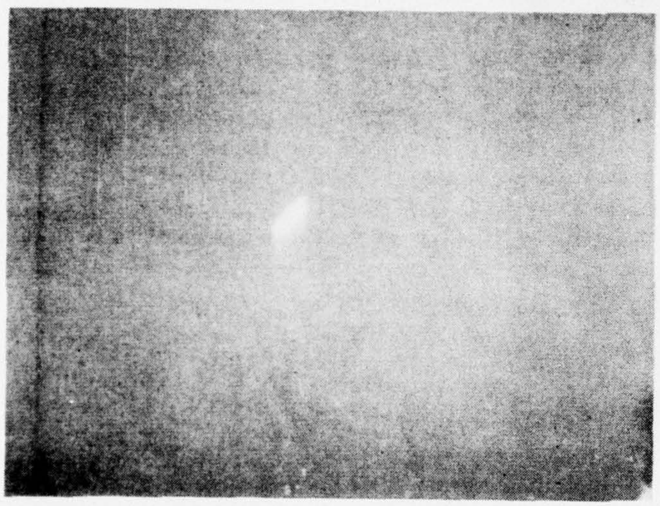


Figure C21c. Light slit positioned horizontally.

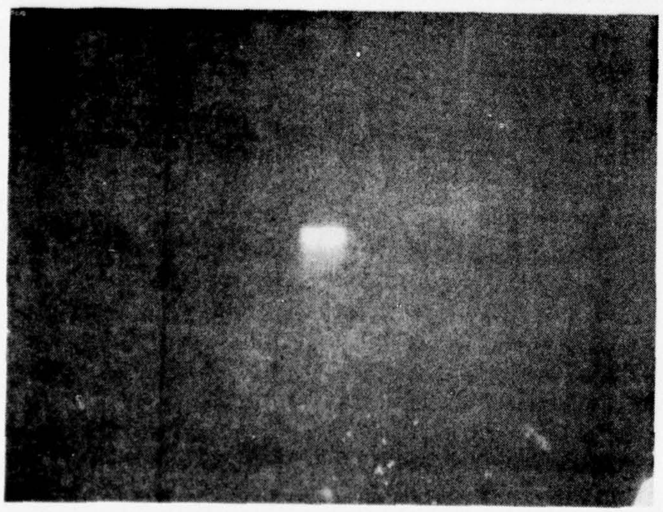


Figure C21d. Light slit positioned over the junction of adjacent pels.

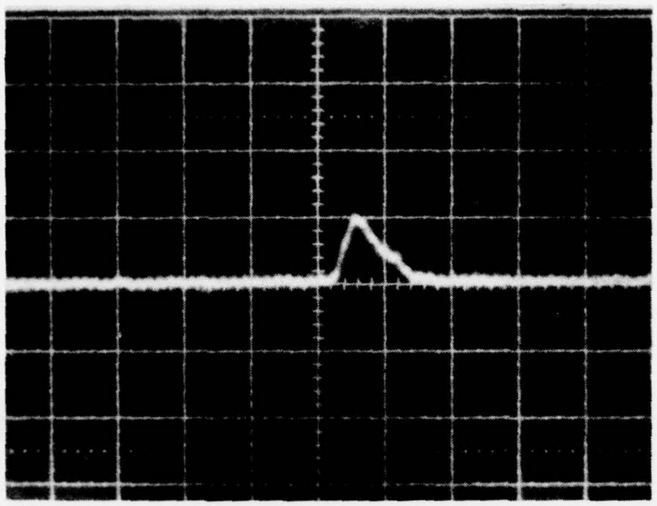


Figure C22b. Video signal for C21b.

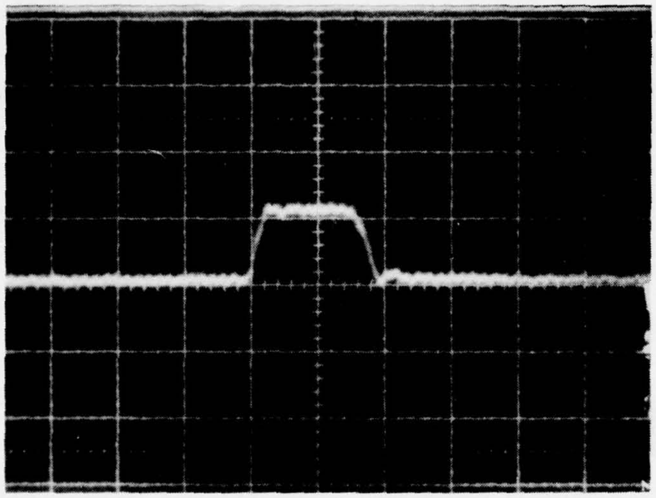


Figure C22c. Video signal for C21c.

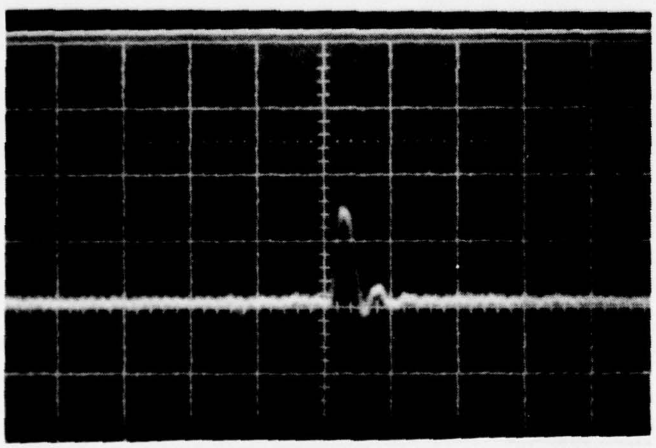


Figure C22d. Video signal for C21d.

BLEMISHES

All test signals were removed and the TV monitor brightness and contrast controls were adjusted to look for imager blemishes. Figure C23 shows the results. None of the blemish areas appears to be completely dead—just less sensitive than adjacent areas. Even the solid dark vertical line yields light. No oscilloscope pictures were taken showing the blemishes because it was virtually impossible to isolate them for photographic record.

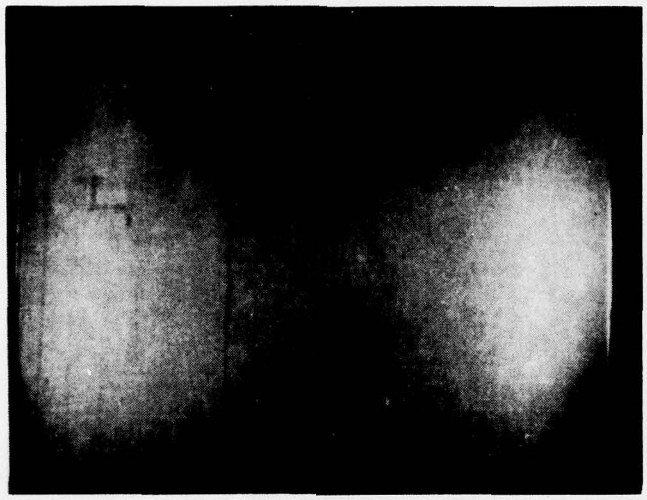


Figure 23. Blemishes on the CCD imager as seen on a TV monitor with no other signal present and the monitor brightness set higher than normal.

COLOR SENSITIVITY

Some interference filters were put into the microprojector to simulate red, green, or blue radiation that may be required to maximize the contrast between various inks and papers. With no test target in the projector, the TV monitor brightness was noted to be quite uneven, and this unevenness changed with the color of radiation that was flooding the CCD imager. In order to further check out this characteristic, a Bausch and Lomb High-Intensity Grating Monochromator was used to flood the imager with essentially flat illumination. The slits in the monochromator were set to give a half-power bandwidth of about 20 nm. Figures C24, C25, and C26 show the TV monitor results and the associated video waveforms for red, green, and blue light, respectively. The “b” photographs are of all the video between vertical sync marks, and the shape is representative of the camera sensitivity change from top to bottom of the imager. The thickness of the line is representative of the variation in sensitivity going across the screen. The “c” photographs show the horizontal variation near the middle of the picture.

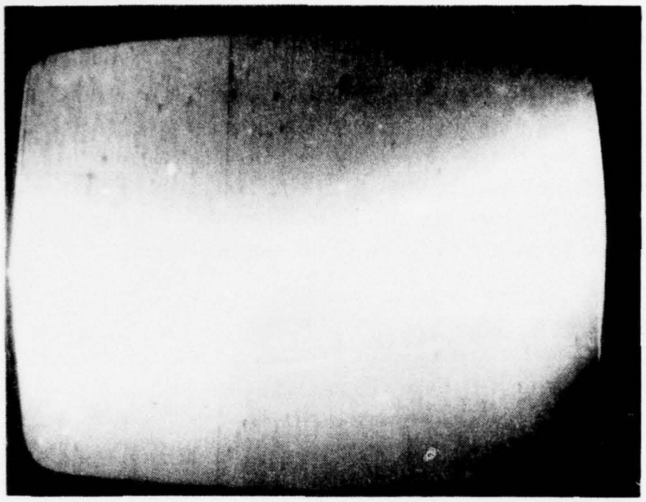


Figure C24a. RCA CCD camera response to 630-nm red illumination.

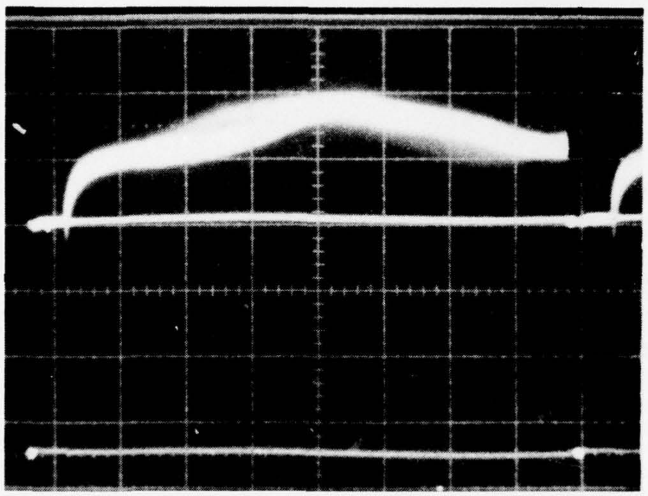


Figure C24b. Video signal between vertical sync pulses that produces the image in C24a.

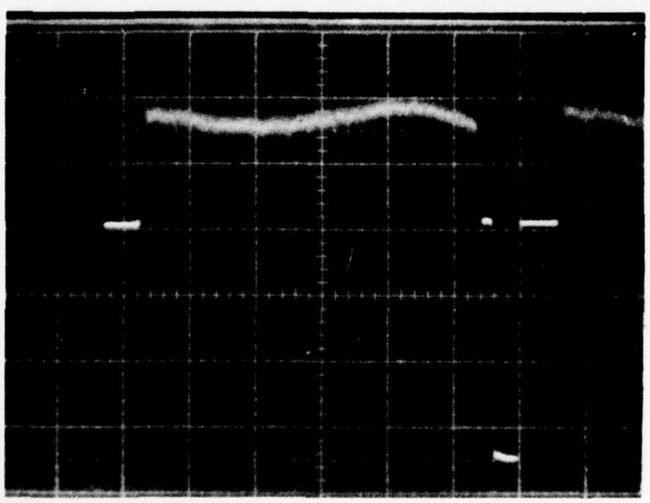


Figure C24c. Video signal for one horizontal line near center of C24a.

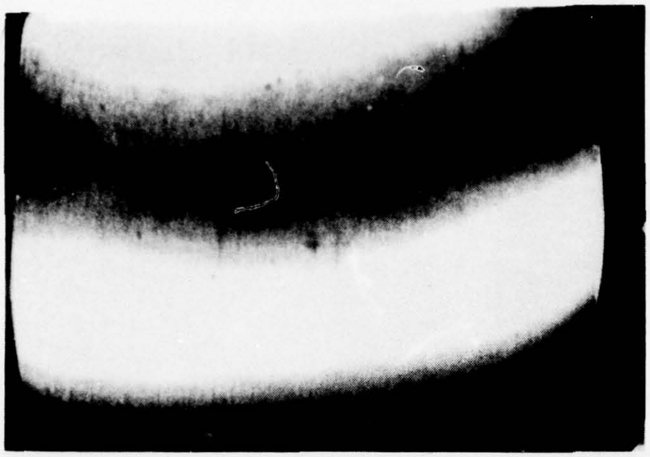


Figure C25a. RCA CCD camera response to 530-nm green illumination.

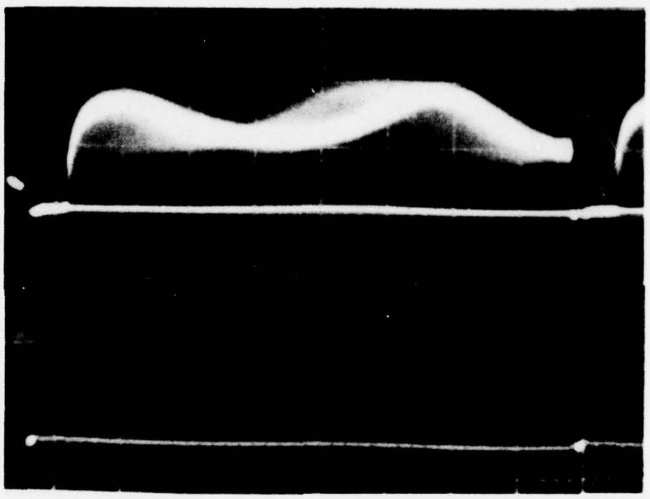


Figure C25b. Video signal between vertical sync pulses that produces the image in C25a.

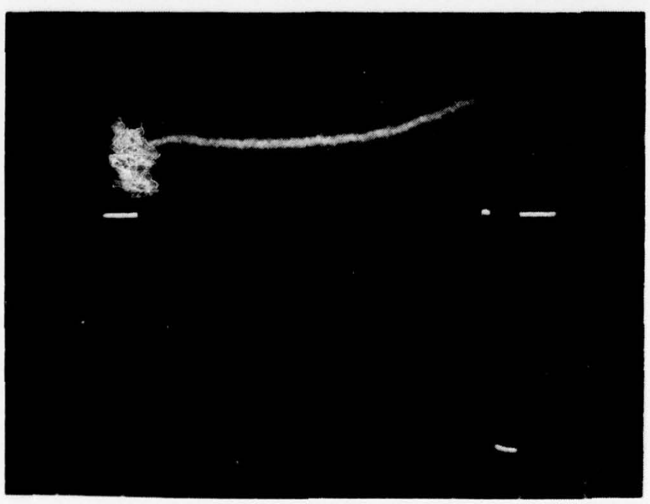


Figure C25c. Video signal for one horizontal line near center of C25a.

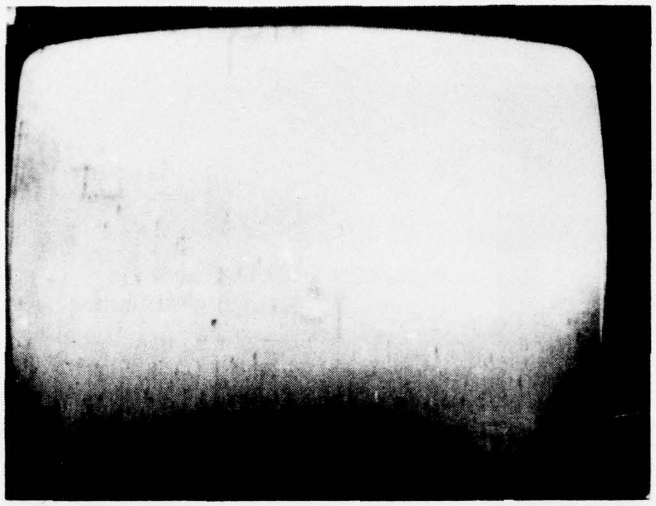


Figure C26a. RCA CCD camera response to 430-nm blue illumination.

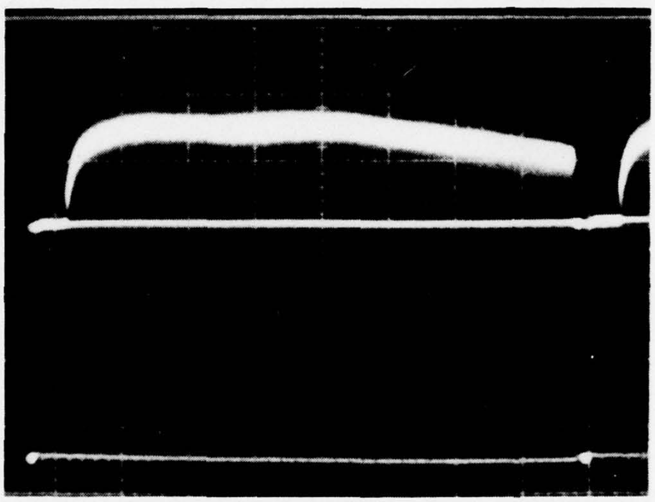


Figure C26b. Video signal between vertical sync pulses that produces the image in C26a.

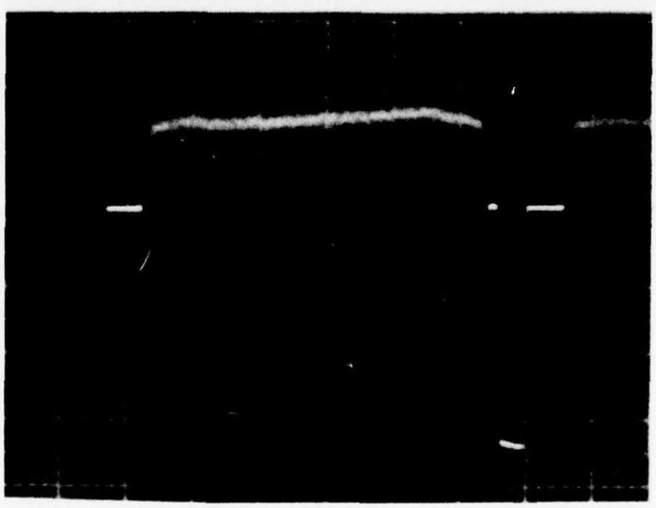


Figure C26c. Video signal for one horizontal line near center of C26a.

IMAGER BIASING

The RCA camera has two red light-emitting diodes (LEDs) positioned on each side of the imager active area. These LEDs optically bias the imager (with "fat zero") to a level that results in satisfactory performance. No attempt was made to prove that RCA had made the optimum adjustment, but considerable effort was expended in characterizing the camera performance with and without the biasing.

Figure C27 shows the compiled results of the testing. The absolute value of maximum light input was not measured but was the same for all four curves shown. Curve 1 appears to be the best. It was taken without any bias illumination, but it is of no use because it was the result of flooding the entire chip with white light. In effect, it shows the response of the chip to a bias that takes the chip from zero output to saturation. Within the accuracy of the measurement techniques, the device is linear. (Linear response plots as a straight line on log-log paper.)

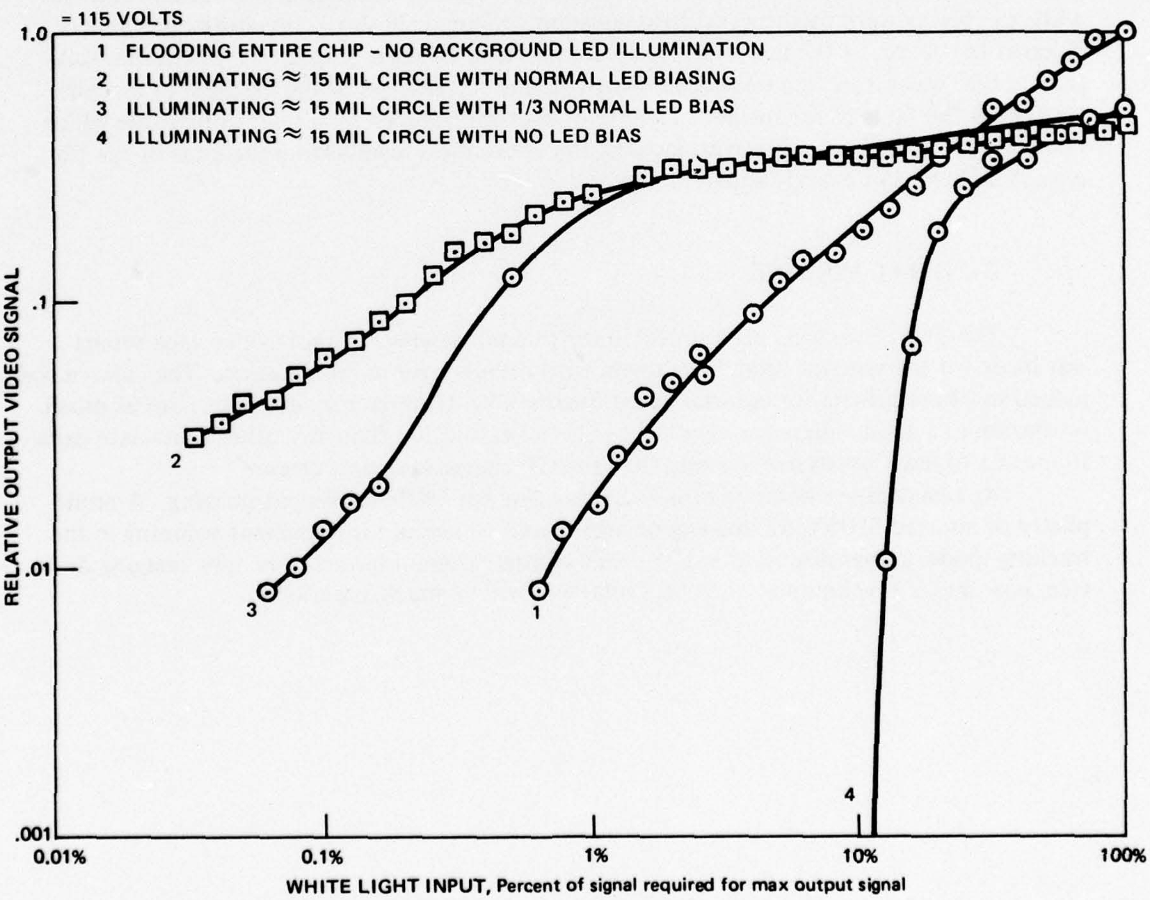


Figure C27. RCA silicon imaging device camera, video output as a function of white light input.

Curves 2, 3, and 4 are the more practical ones, as they show the performance when a small area of the imager receives illumination with different amounts of LED bias present. Perhaps the most significant point these three curves show is that a small area saturates at a lower video output level than a larger area does. This is attributed to adjacent pel loading effects. Conversely, it is also noted in testing the imager that a small dark area in a large bright background will not yield as large a dip in the output video level as a larger dark area would. Taking the curves individually, the performance represented by curve 4 (no background bias was used) is of no use. The imager has no dynamic range. The performance represented by curve 3 (about 1/3 normal bias used) appears to have acceptable dynamic range. However, it saturates with a more pronounced characteristic than when full bias (as determined by RCA) is used, as represented by curve 2. Although it was possible to increase the bias above the normal setting, it could not be raised enough to make another curve. It does appear, however, that the bias level chosen by RCA is near optimum for most purposes.

In addition to the data presented in figure C27, there is another reason why performance of the imager is not acceptable when the background bias is reduced significantly or eliminated completely. This reason is shown rather dramatically in figures C28a through C28h. Figure C28 shows how the TV monitor image is affected by decreasing the background bias while the test pattern brightness is held constant. Figure C29 shows one horizontal line of video at the center of the test spot. They are included to show graphically where the background bias was set for the respective TV image and unevenness of the bright spot in figure C28 is not the fault of the imager. The bright spot is produced by a fiber optic cable which has a few broken fibers. However, most of the unevenness results from the ends of the fibers not all being cut exactly square.

GENERAL VIEWING

The TC115 camera was also tested for general viewing. A short video tape report was made for the sponsor using the camera with ordinary room illumination. The camera was judged to be acceptable for entertainment quality TV. It, of course, does not have as much resolution as a good vidicon camera but has better resolution than any other solid-state camera. It appears to have less dynamic range than the GE charge injection cmera.

As a camera the equipment is not applicable for USPS document imaging. A multiplicity of abutted SID51232 imaging devices would be useful for document scanning in the tracking mode, as was discussed in last year's annual program report. The new imaging device, now under development at RCA, Princeton, will be much superior.

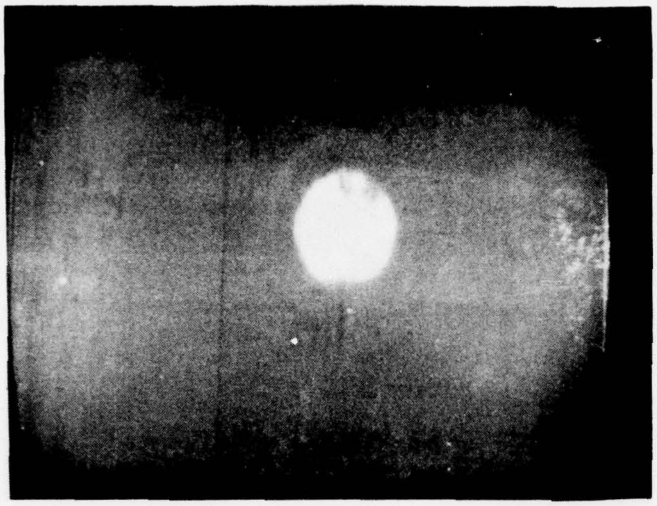


Figure C28a. RCA CCD camera response to a bright spot on a dark background at full background bias. Figures b through e are for reduced levels of bias illumination. Figures f through h show camera response to a dark spot on a bright background with decreasing levels of background bias.

Figure C28b.

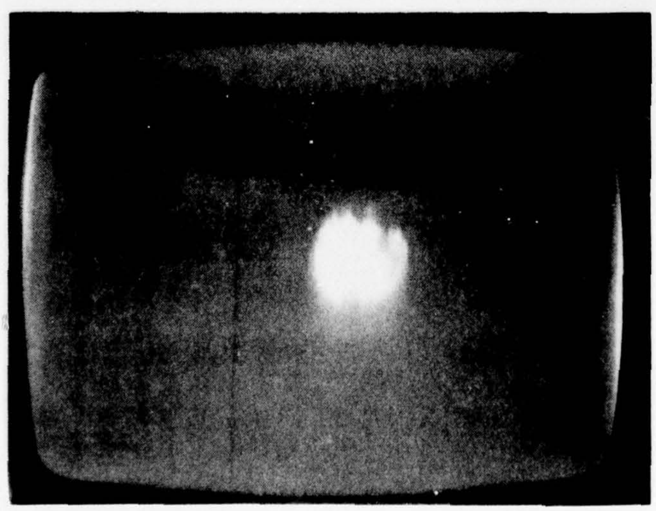


Figure C28c.

Figure C28d.

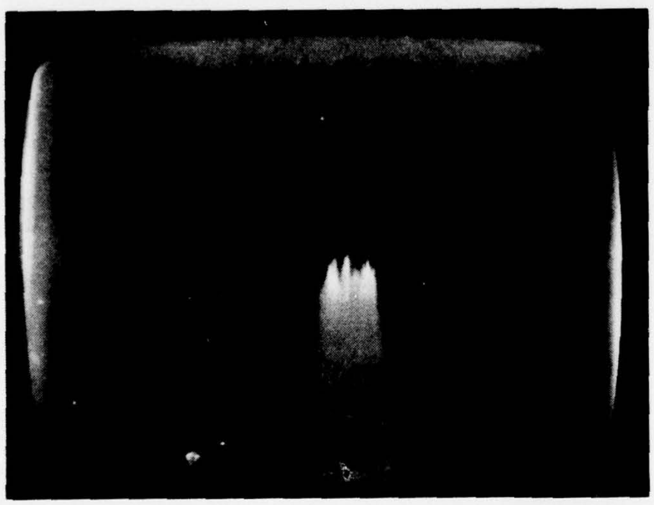


Figure C28e.

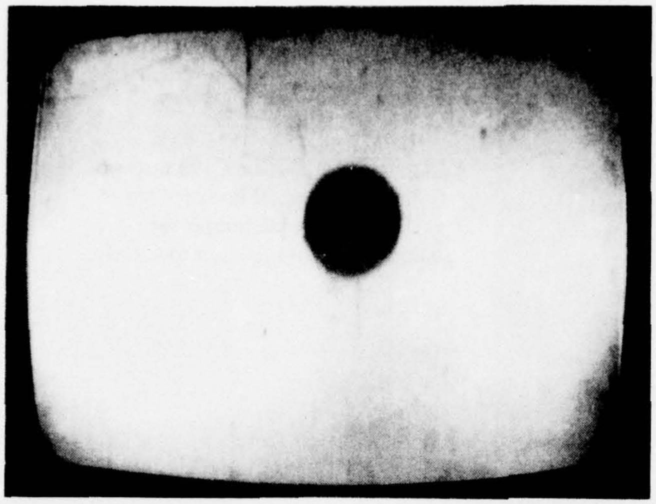


Figure C28f. Full background bias illuminztion.

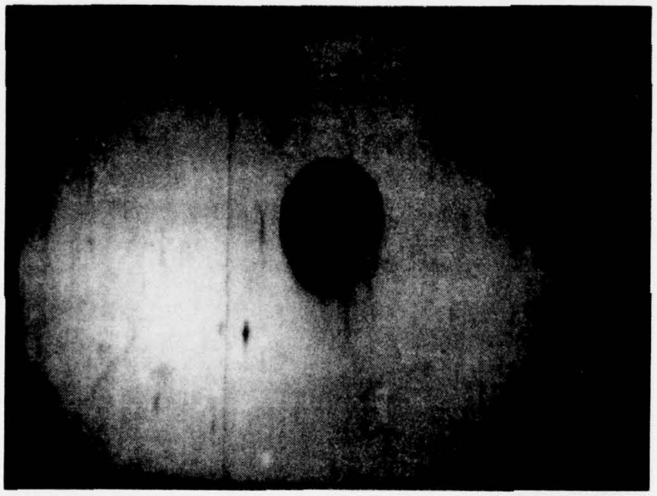


Figure C28g.

Figure C28h.

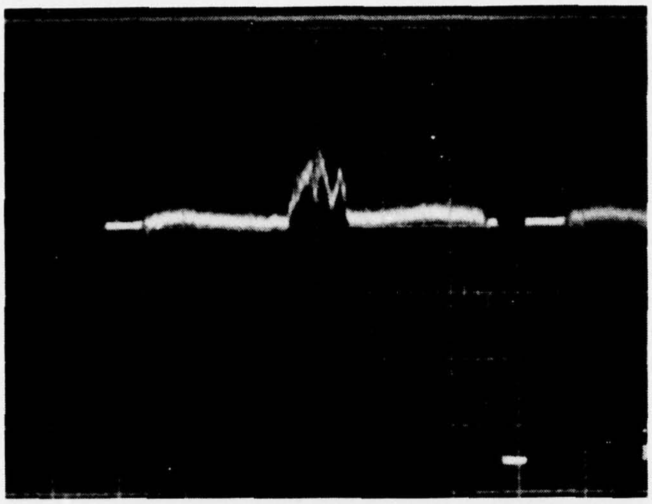


Figure C29a. Figures C29a through h show a horizontal line of video at the center of the images for figures C28a through h, respectively.

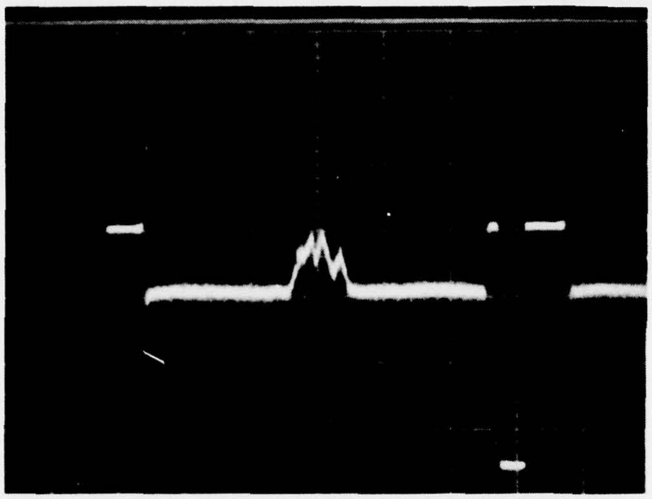


Figure C29b.

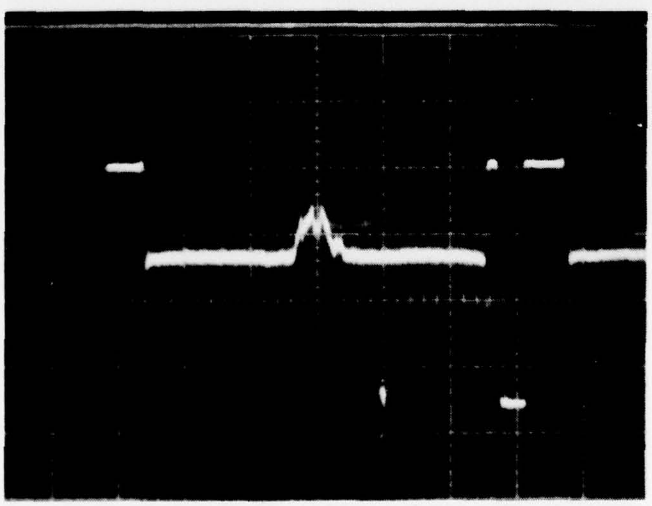


Figure C29c.

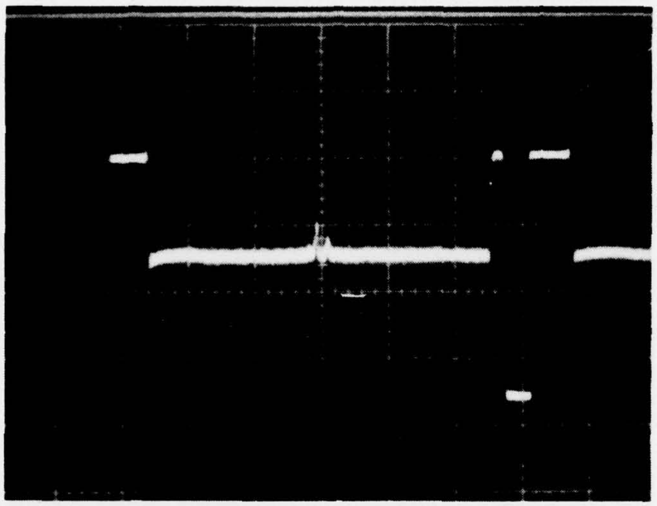


Figure C29d.

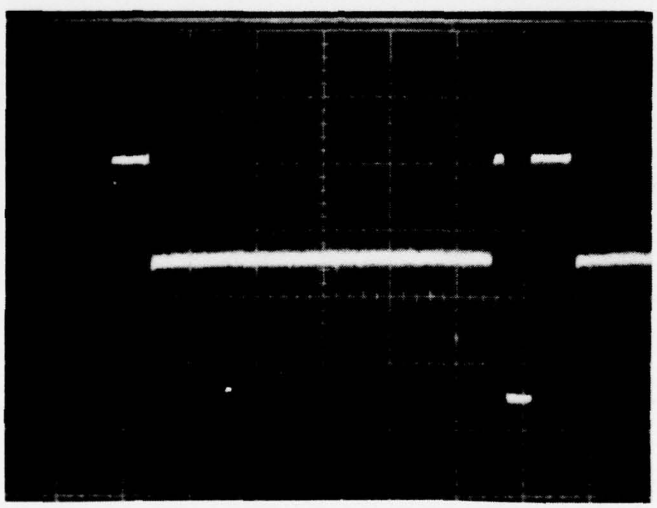


Figure C29e.

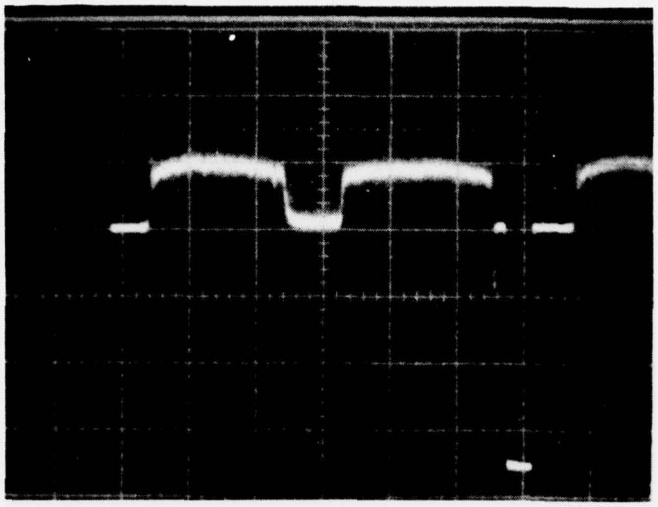


Figure C29f.

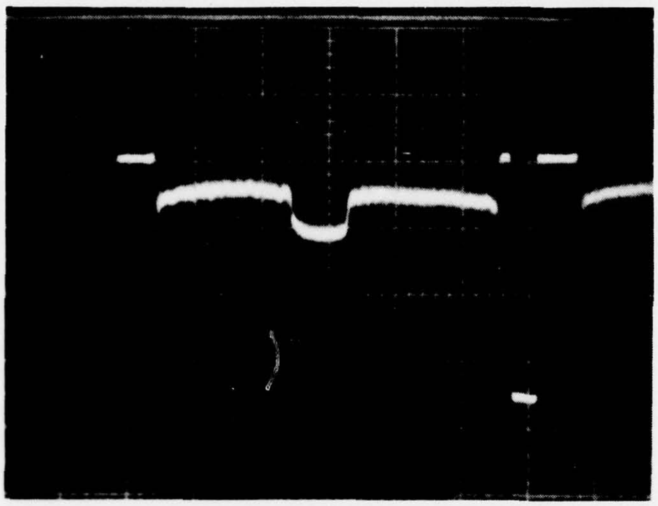


Figure C29g.

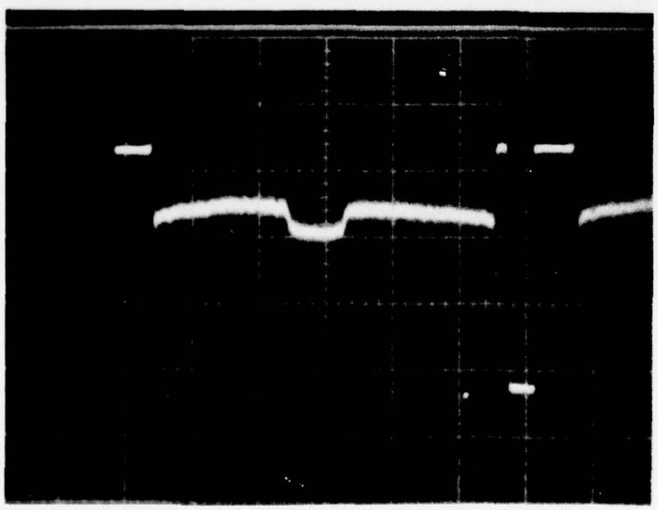


Figure C29h.

TRACKING IMAGER TESTS

INTRODUCTION

The Advanced Mail Systems Scanner Technology First Annual Report discusses the advantages of a "tracking" imager both in increased resolution in the direction of copy motion and in optical sensitivity. Also included in the report were recommendations to pursue investigations into abutting two or more of the RCA SID51232 devices to obtain a wider image than the 320 pels available from a single imager.

Doctors Walt Kosonocky and Jim Carnes of RCA, Princeton, felt that it is possible to design and fabricate a single device which will meet all the present Postal Service requirements. These requirements include:

1. At least 1700 (and preferably an option of 2200) pel resolution normal to the direction of copy motion.

2. An output rate of 84 megapels per second preferably from at least four ports, with each concurrent output providing data on four or more adjacent pels.

3. Operation in the tracking mode to improve resolution and optical sensitivity.

RCA has submitted an unsolicited proposal to NELC (p75-115, RCA Princeton, 12 December 1975) to design, fabricate, test, and deliver working samples of devices which will verify the level of achievement of the above goals. NELC has accepted the proposal, and a contract (N00123-76-C-0980, 15 March 1976) has been awarded. RCA will design and fabricate a number of prototype devices having at least 750 elements in the horizontal direction (normal to copy motion) and up to 100 elements in the vertical (tracking) direction. These will be completely characterized by the RCA staff. At the termination of the tests, the data, any support electronics, and 10 of the devices will be delivered to NELC (about 15 March 1977) for further studies on the program.

THEORY OF OPERATION

The theory pertaining to tracking imager advantages was covered in last year's annual report, but will be repeated here because of its relevance to the best approach we have devised to achieving the USPS imaging goals.

A device such as the RCA SID 51232 can be controlled while accumulating photon-generated electron charge packets of data to transport the potential wells in synchronism with the projected moving image impinging on the array. In addition to the advantage of a longer integration time and the lack of a requirement for concentrated illumination, the resolution which can be obtained in the direction of copy motion is substantially improved. The achievable improvement in resolution which can be made by using a tracking imager can be seen in figure C30. On the left side of the figure a standard line imager such as the Fairchild CCD110 is presented. On the right side a tracking imager having a three-phase clock such as the RCA SID51232 device is presented. The figure shows (from top to bottom) the acquisition cycle for two cells of data from each of the two types of imagers. A cell in this case is meant to be one complete line of data shifted from the CCD device in the case of the line imager. In the case of the tracking imager, one cell is meant to be one family of three phases of image data being transported in the direction of the impinging

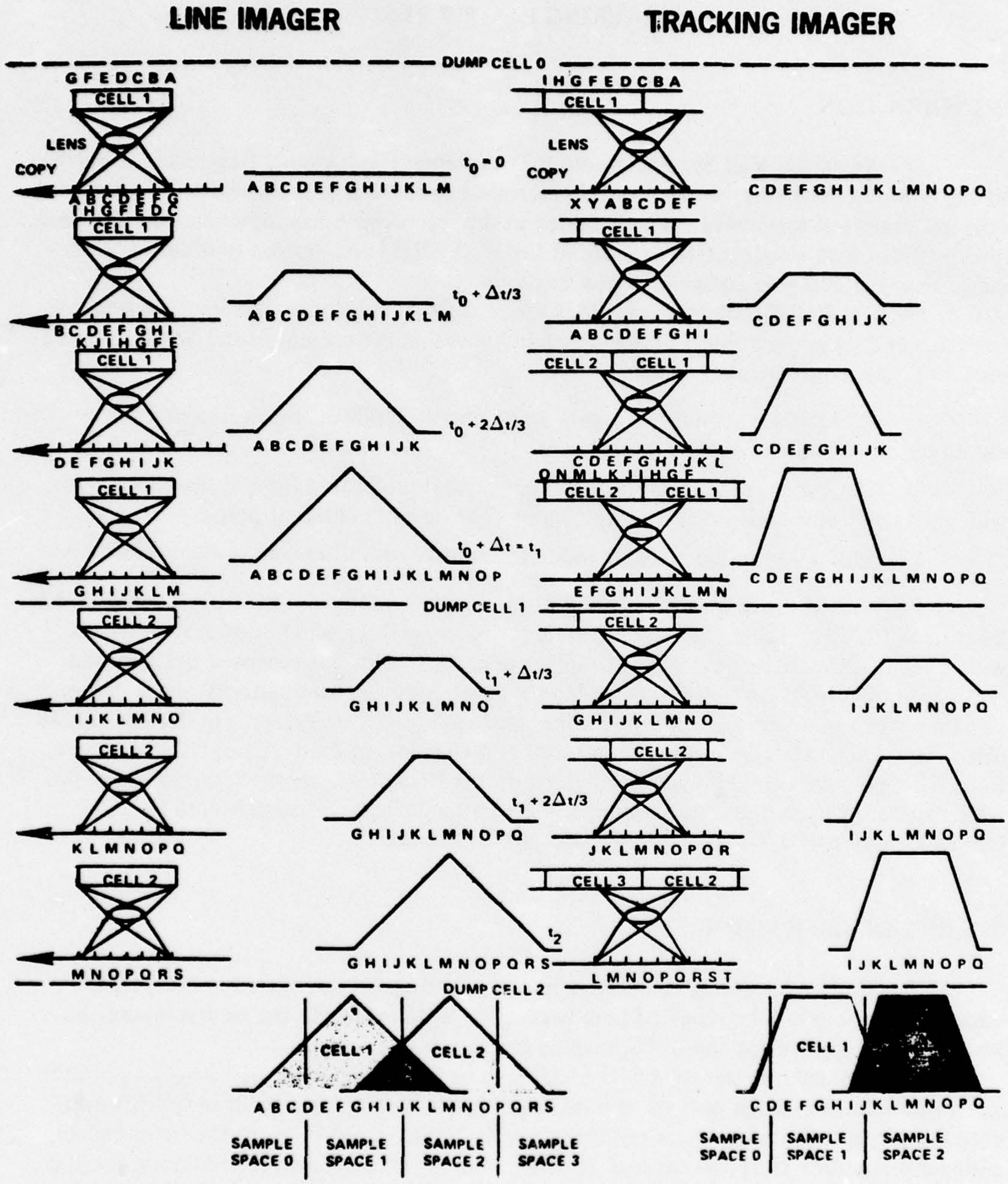


Figure C30. Resolution advantages of a tracking imager.

image along the device. The sequence of small pictorial diagrams from top to bottom on the left hand side of the page depicts the motion of copy during each one-third of a line sample interval. In the next column to the right of these sketches the accumulation of charge within the cell is diagrammed. These increasing charge diagrams verify the process of the convolution integral of the imager with a rectangular aperture and an equivalent area of projected information from the copy below.

The accrued charge in cell one at time $t = t_1$ is the familiar triangle resulting from convolution of two rectangular areas. It can be seen that the contributions to the charge under the triangle have come from image points ranging from A through M on the copy, with the maximum point occurring at image point G. This is because point G was the only point to contribute continuously to the illumination of the cell throughout the entire period from t_0 to t_1. Location A on the copy moved from the field of view of cell one immediately after the cell was dumped from the previous scan, and point M moved into the field of view just as cell one was dumped.

What is depicted at cell two is, of course, the same imager being photoactivated again during the interval between t_1 and t_2 after being dumped at t_1. The same familiar triangular waveform from the convolution is present, with the point M on the copy being at the highest point during this scan period. At the bottom of the figure the true apertures of cell one and cell two are plotted to show the overlap which exists between cell one and cell two (the cross-hatched area). That portion of the cell-one area which lies in sample space two (which is 12½% of the area under the cell-one curve) actually lies in sample space two. Another 12½% of the cell-one area actually lies in sample space zero. Therefore, 25% of the cell-one output has no relationship to the information within sample space one at all, but rather is an erroneous reading of information actually acquired in sample space zero and sample space two. One method of preventing this overlap is to double the line scan frequency, which in turn oversamples the information normal to the direction of copy motion by a factor of 2:1. This also doubles the CCD output rate requirement, which is already a formidable 83 megapels per second.

A similar pair of sequential drawings is shown on the right side of the page for the tracking imager. The tracking imager has the ability to move the location of the accumulating photo sites and potential wells to the right in this picture in three discrete steps per sample time interval in synchronism with the motion of the copy image on the device. Integration starts with the copy and cell as shown in the top figure. As the copy moves to the left, image point C on the copy projects an image which passes to the right and out of the view of cell one. Therefore, no contribution from image point C is contained in cell one. Information from point D, however, and point E projects progressively longer onto cell one before the copy has moved far enough that the image is beyond the view of cell one. Therefore, the accumulated image data in cell one at $t_0 + \Delta t/3$ is the same for the tracking imager as it was for the line imager. At this point the operation of the tracking imager diverges from that of the line imager. At $t_0 + \Delta t/3$, the clock phases of the potential well of cell one are changed so that the cell moves by an increment of one-third line scan interval. By design, this is exactly the same distance that the projected image of the copy had moved during the first interval. Therefore, during the time between $t_0 + \Delta t/3$ and $t_0 + 2\ \Delta t/3$, the same optical relationship remains which existed during the first one-third interval, and the acquired image data will relate to exactly the same points on the copy as during the first interval. Consequently, the convolution waveform appears to be exactly like the one above it except that it now has twice the amplitude.

At just after time $t_0 + 2\ \Delta t/3$ the potential wells of the tracking imager device are again shifted by one-third sample space and the image is caused to sweep over the same

one-third increment for the third time, providing a final convolution waveform which appears three times the amplitude of the first increment.

After cell one has been dumped or carried forward for further integration into a final output shift register, a second cell immediately following the first begins to acquire data on subsequent points on the copy space. The buildup of photosensitive charges is shown for cell two immediately below cell one.

Again at the bottom of the figure, cell-one and cell-two waveforms are shown side by side, again indicating the overlap between the two cells. This time the overlap is dramatically reduced by a factor of 3:1 so that the total contribution is only approximately 4% from sample space two into cell one; and second, the contribution that is made does not deeply penetrate into cell two but extends only one-sixth of the way past the boundary between cell one and cell two. No degradation in response will occur in either type of operation, since the total areas of charge one under the line imager and the tracking imager are identical.

This apparent great improvement in resolution in the direction of copy constitutes a deblurring advantage only if the tracking imager can be made to follow exactly the projected image of the copy on the imager photosensitive area. The sample spaces shown at the bottom of the page represent physical dimensions on the copy of only 0.005 inch each. The distance between the letters I and J in sample space one represents only 0.00083 inch. If the tracking imager cannot be controlled to follow the copy image to approximately this accuracy, the only remaining advantages of broader illumination latitude and longer integration time will have to be examined to determine the cost-effectiveness of exploiting a tracking imager.

NEAR-TERM TEST PLANS

Both the government and RCA, Princeton, are anxious to evaluate the concept of tracking imaging as applied to Postal image acquisition. RCA (and others in CCD development work) refer to this technique as the time-delay-integration (TDI) mode. One of the important near-term goals of the program is to run meaningful tests with available equipment which will assist in the design decisions of the devices now under contract to RCA.

CAMERA MODIFICATIONS

There are a number of modifications required in the RCA TC1155 camera for operation in the tracking (TDI) mode. A decision has been reached to utilize the internal 15.75-kHz clock signal as the three-phase tracking mode clock frequency. The alternatives were to change the internal oscillator frequency to 48.0 kHz to match our maximum design goal acquisition rates or to provide for external input of a variable or drum controlled clock. A terminal which will provide the 15.75-kHz output signal will be added to the camera. It is also necessary to modify some of the gate control signals into or out of the SIDA 1002 analog switch IC so that the 15.75-kHz clock signals are provided to the "ΦB" lines continuously during tracking operations.

A physical disassembly of the camera is necessary in order to illuminate the half of the SID51232 imager device normally used for storage. The front face containing the

lens mount will be carefully removed and an alternate lens holder will be substituted. It would be possible to use the regular imaging area of the SID51232 if the "ΦA" three-phase clock leads were also switched to the 15.75-kHz continuous signal, but if this were done the tracked signals would be required to pass through the additional 256 storage stages of the vertical CCDs in order to reach the output horizontal register. Better signal quality should be obtained by using the stages immediately adjacent to the output horizontal register for the optical imaging.

Some additional modifications are being made to the camera in order to evaluate some proprietary RCA devices in the tracking mode. These are described in the proprietary appendix (TR 2020 v 2, available to US Government agencies only).

TEST SETUP

The ideal test setup for tracking imager studies would include a facility for carefully controlled linear motion of flat pages of test copy. Neither of the NELC test beds can accommodate this feature, although some thoughts have been given to providing a "belt" of 70-mm photographic film copy for the SDTB which could be mounted in conjunction with an idler pulley to provide a limited flat bed capability. By back lighting the film through an opal glass suspension shoe (like a belt sander) and obtaining synchronizing impulses from the sprocket holes which can be ratio matched on a dual-beam scope with the 15.75-kHz pulses, a somewhat marginal setup can be obtained.

The problems of tracking copy mounted on a curved drum surface are related to the geometric distortions of the X and Y apparent motions of portions of the image as seen from the lens position. These distortions decrease as a function of increased drum diameter and increase as a function of height of image space used in the optical acquisition process in the direction of copy motion.

Appendix D (to this appendix) shows the equations related to the aberrations generated by the curved object surface. It also shows by the three examples that by using 100 pels or less in the direction of copy motion, the errors in vertical and horizontal nonlinearity are not greater than 40% of a pel area. Example 3 in this appendix also indicates that even the SDTB can be used to obtain meaningful measurements with the TC1155 Camera in the tracking mode. It should be pointed out that the errors are a function of the location of the optically unmasked and illuminated area, so that verification of the calculated aberrations and their cosmetic effects on acquired images can be studied for a variety of numbers of pels used in the direction of tracking.

SOLID-STATE IMAGER STATUS

At the end of last year's program, a table (table C2) was provided in the annual report. It included all known off-the-shelf solid-state imaging devices which could be relevant to USPS imaging applications. This table is being included unmodified in this report. Only two new devices of any significance have been developed this year, and data sheets have not been made available on these as yet. One device is a 1728-bit line imager from Reticon. The other is a Fairchild area imager having 380 and 488 pels in width and height, respectively.

Neither of these imagers would change the ranking of choices on table C2. The time-delay integration imager now under contract at RCA, Princeton, of course, now outranks all other candidates on the table, since it will be designed specifically for high-speed tracking of USPS copy material

TABLE C2. RELATIVE APPLICABILITY OF VIDEO SENSORS FOR

	Manufacturer	Device Type Number	Array Size, pels	Element Spacing mils	Element Size, mils X mils	Data Rate min kKz	Data Rate max MHz	Sensitivity fc•s $\mu Ws/cm^2$	Saturation Exposure fc•s $\mu Ws/cm^2$	Uniformit of Sensitivity %
Linear Devices	Reticon	RL-512B	512 X 1	1.0	1.0 X 1.0	10	40	7×10^{-4} 3.5×10^{-2}	7×10^{-2} 3.5	±7
	Reticon	RL-1024B	1024 X 1	1.0	1.0 X 1.0	10	40	7×10^{-4} 3.5×10^{-2}	7×10^{-2} 3.5	±7
	Reticon	RL-1872F	1872 X 1	0.59	0.59 X 0.63	10	20	13 pa/ft cdl 0.26 pa/μW/cm^2	0.246 12.3	±12
	Fairchild	CCD-101	500 X 1	1.18	1.0 X 1.0	10	1.1	3.0×10^{-5} 1.5×10^{-3}	15×10^{-3} 0.75	±15
	Fairchild	CCD-110	256 X 1	0.51	0.51 X 0.63	10	10	9.0×10^{-5} 4.5×10^{-3}	9×10^{-3} 0.45	±10
	Fairchild	CCD-121	1728 X 1	0.51	0.51 X 0.67	10	1.0 typ.	5.9×10^{-5} 2.9×10^{-3}	10^{-2} 0.5	±10
	AMERCON	proposed	1728 X 1	5	3 X 5	0	0.085	?	?	requires calibratio adjustme
Area Devices	Reticon	PA 50 X 50A	50 X 50	4.0 X 4.0	8 mils^2	10	5	250 pa/ft cdl 5 pa/μW/cm^2	3×10^{-3} 0.15	±10
	Fairchild	CCD-201	100 X 100	1.2V X 1.611	1.2 X 0.8	100	4	1.6×10^{-5} 0.8×10^{-3}	3.1×10^{-3} 0.16	±15
	RCA	SID 51232	512 X 320	1.2 X 1.2	1.2 X 1.2	10	6.1 typ.	2.9×10^{-5} 1.4×10^{-3}	2.67×10^{-3} 0.13	±10 est
	RCA	2½" RBV	3000 X 3000	0.3	0.3 X 0.3	0	85	10^{-4} 5×10^{-3}		±10 est
	RCA	4" RBV	6000 X 6000	0.3	0.3 X 0.3	0	85	10^{-4} 5×10^{-3}	10^{-2} 0.5	±10 est
	GE	Z 7892	188 X 244	1.4 X 2.4	1.4 X 2.4	10	4	1.1 μa/ft cdl 60 ma/W/cm^2	.45 8 - 8.5	±10 est

APPLICABILITY OF VIDEO SENSORS FOR ELECTRONIC MESSAGE SERVICE.

Sensitivity fc•s $\frac{\mu Ws}{cm^2}$	Saturation Exposure fc•s $\frac{\mu Ws}{cm^2}$	Uniformity of Sensitivity %	Dynamic Range			Spectral Response nm	Output Amplitude volts, max	Abutment Problem	Remarks	Relative Applicability Rank
			min	type	max					
7×10^{-4} 3.5×10^{-2}	7×10^{-2} 3.5	±7		100		400 - 1100	0.04	moderate 3 linear abutments	output available from four parallel video lines	5
7×10^{-4} 3.5×10^{-2}	7×10^{-2} 3.5	±7		100		400 - 1100	0.04	minimum 1 linear abutment	output available from four parallel video lines	4
pa/ft cdl 6 pa/μW/cm^2	0.246 12.3	±12		100		400 - 1100 (900 peak)	0.06	none	output available from four parallel video lines	3
3.0×10^{-5} 1.5×10^{-3}	15×10^{-3} 0.75	±15	200		500	500 - 1000	0.5	moderate 3 linear abutments	speed limits applicability would require 80 devices	–
9.0×10^{-5} 4.5×10^{-3}	9×10^{-3} 0.45	±10	200		400	400 - 1100	0.05	difficult 7 linear abutments	waveforms of output vs noise are excellent	2
5.9×10^{-5} 2.9×10^{-3}	10^{-2} 0.5	±10		170		450 - 1050	0.2	none	speed limits applicability – need 80 megapels/s	–
?	?	requires calibration adjustment		100		350 - 800	0.5	none	cadmium sulphide photo-resistor array; much development required	–
50 pa/ft cdl pa/μW/cm^2	3×10^{-3} 0.15	±10			100	400 - 1100	0.032	massive 44 X 34 xy abutments	requires physical abutments plus multiple strobe exposures per page	–
1.6×10^{-5} 0.8×10^{-3}	3.1×10^{-3} 0.16	±15	100		200	480 - 1100	0.075	massive 22 X 17 xy abutments	requires physical abutments plus multiple strobe exposures per page	–
2.9×10^{-5} 1.4×10^{-3}	2.67×10^{-3} 0.13	±10 est	80		100	420 - 1100	0.0125	difficult $6 \rightarrow 13$ linear θ abutments	optimum for lighting requirements; requires tracking of image with CCDs	1 (highest)
10^{-4} 5×10^{-3}		±10 est		100		450 - 1100	current mode operation	none	has resolution, speed & sensitivity; the 0.5-s target prep time bad	–
10^{-4} 5×10^{-3}	10^{-2} 0.5	±10 est		100		peaks in visible with ASDS target	current mode operation	none	has resolution, speed & sensitivity; the 0.5-s target prep time bad	–
μa/ft cdl ma/W/cm^2	.45 8 - 8.5	±10 est		200		400 - 1100	0.5 from preamp	severe 9 X 9 xy abutments	requires physical abutments plus multiple strobe exposures per page	–

FLYING SPOT SCANNERS

INTRODUCTION

Although most of the effort on the program thus far has been applied to solid-state imagers, some investigations were made into the applicability of flying spot scanners. Data obtained from current literature and trips to Dest Data and RCA confirmed that flying spot scanners are applicable to high-speed, high-resolution imaging. At the invitation of the Electro-Optical Group a visit was made to Harris Laboratories in Melbourne, Florida.

HARRIS ELECTRO-OPTICAL CAPABILITIES

At Harris we were given a presentation of the various methods of utilizing flying spot scanners for image acquisition and image recording. The speed and resolution limitations to each were explained. The system applicable to USPS high-speed image acquisition employed a Bragg cell device having a basic resolution of about 1000 lines per sweep. This provided the basic scan deflection. An acousto-optic traveling wave lens would be used in conjunction with a cylindrical lens to further refine the spot size by a factor of 20 times or more to an upper limit of 20 000 to 50 000 resolvable points per sweep. A demonstration of the beam deflection system including the traveling lens indicated an extremely stable mode of operation. Mechanical vibrations were compensated out by action of the traveling lens. The optical path required would be about 2 metres and can be folded into a fairly compact assembly.

From the demonstrations we witnessed and data we were given, it is evident that flying spot scanner technology is a candidate approach for USPS imaging. More data regarding relative costs, support electronics, and mechanical rigidity will be needed to provide comparative system advantages.

SUMMARY AND CONCLUSIONS

1. Circuit design has been completed which will compensate for image brightness irregularities caused by nonuniformity of illumination, optical path, and device response.

2. The RCA solid-state camera has been characterized for static imaging.

3. Limited tracking mode tests can be made with the RCA camera on the large drum scanner test bed.

4. Early tests of the RCA camera in the tracking mode will assist in the establishment of parameters of the new RCA imager.

5. If successful, the RCA device development will establish the technology and architectural design of a single imaging device which will meet all the US Postal Service imaging goals.

6. The large drum scanner test bed now provides a facility with which precise, repeatable imaging measurements can be obtained.

7. The large drum scanner test bed is now interfaced with the frame store memory controller and the image analyzer, which are in turn interfaced to the Kennedy tape deck and the Tektronix keyboard terminal.

8. Flying spot scanner technology appears to have applicability to USPS imaging.

FUTURE NELC PLANS

1. Evaluate the necessity for (or degree of) image brightness compensation by software program in the memory controller.

2. Acquire a fully compensated 8½-by-11-inch image having 200-by-200-pel resolution and full 6-bit Gray scale on tape.

3. Provide a program using the Kennedy tape deck (and the GFE Bright tape deck) to subdivide the acquired image into sub-pictures which can be stored in the frame store memory and displayed on the Conrac monitor.

4. Using the test bed, take the data for the image compressibility study. Reduce the data and generate the summary report.

5. As schedule permits, instrument the RCA camera and the large drum test bed to perform limited image tracking experiments.

6. Convey the resulting information to RCA, Princeton, and discuss applicability of findings to the new image design.

7. Following these milestones, begin the image enhancement studies using the test bed and software algorithms.

APPENDIX A (TO TR 2020 APPENDIX C);

ILLUMINATION UNIFORMITY TEST DATA

FULL SCALE WIDTH

Position Across Drum, Inches	Relative Intensity Output, Millivolts	Repeated Readings, Millivolts	Average, Millivolts	Normalized Values
2.0	86.0		86.0	0.563
2.5	98.2		98.2	0.643
3.0	114.6		114.6	0.75
3.5	128.0		128.0	0.838
4.0	135.2	139.0	137.1	0.897
4.5	153.2	152.5	152.8	1.000
5.0	155.0	154.5	154.8	1.013
5.5	158.9	159.8	159.4	1.043
6.0	152.6	153.1	152.8	1.000
6.5	155.6	154.3	155.0	1.014
7.0	148.4	148.7	148.6	0.973
7.5	145.9	146.1	146.0	0.956
8.0	148.4	149.3	148.9	0.974
8.5	142.5		142.5	0.932
9.0	134.1		134.1	0.878
9.5	126.6		126.6	0.828
10.0	115.1		115.1	0.753
10.5	110.0		110.0	0.720

ILLUMINATION UNIFORMITY TEST DATA

VERTICAL PROFILES

Height Above Deck, Inches	4.5 Inches From End			6.0 Inches From End			7.5 Inches From End		
	mV	First Norm	Second Norm	mV	First Norm	Second Norm	mV	First Norm	Second Norm
2.42	61.1	0.374	0.358				72.1	0.467	0.423
0.44	83.0	0.508	0.487	99.0	0.589	Same	95.0	0.612	0.554
0.46	109.5	0.670	0.642	122.3	0.728	As	121.0	0.780	0.706
0.48	138.6	0.848	0.812	146.7	0.873	First	140.3	0.905	0.819
2.50	163.4	1.000	0.958	168.0	1.000		155.1	1.000	0.905
0.52	172.6	1.056	1.012	172.0	1.024		162.4	1.047	0.948
0.54	165.0	1.009	0.967	162.7	0.968		161.2	1.039	0.940
0.56	158.1	0.968	0.927	151.8	0.904		152.8	0.985	0.891
0.58	139.1	0.851	0.815	134.8	0.802		134.8	0.869	0.786
0.60	125.7	0.769	0.737	120.1	0.715		117.5	0.758	0.686

ILLUMINATION UNIFORMITY TEST DATA

Distance, Horiz	Intensity, mV	Norm Value	Intensity, mV	Norm Value	5 Mar 76
2.0	83.9	0.522	–	–	
2.5	102.0	0.635	–	–	
3.0	115.0	0.716	–	–	
3.5	131.5	0.818	–	–	
4.0	142.1	0.884	–	–	
4.5	153.9	0.958	–	–	
5.0	156.0	0.971	155.2	0.982	
.1			155.8	0.986	
.2			160.1	1.013	
.3			155.8	0.986	
.4			160.8	1.018	
.5	163.0	1.014	162.2	1.027	
.6			161.7	1.023	
.7			158.6	1.004	
.8			158.9	1.006	
.9			159.9	1.012	
6.0	160.7	1.000	158.0	1.000	
.1			157.9	0.999	
.2			154.7	0.979	
.3			155.7	0.985	
.4			153.0	0.968	
.5	157.8	0.982	156.8	0.992	
.6			148.8	0.942	
.7			154.0	0.975	
.8			147.4	0.933	
.9			150.2	0.951	
7.0	146.3	0.910	145.8	0.923	
.1			151.2	0.957	
.2			149.0	0.943	
.3			146.9	0.930	
.4			149.4	0.946	
.5	145.4	0.905	148.0	0.937	
.6			151.9	0.961	
.7			145.0	0.918	
.8			147.3	0.932	
.9			146.0	0.924	
8.0	152.0	0.946	151.5	0.959	
.1			144.1	0.912	
.2			143.3	0.907	
.3 .3			142.9	0.904	
.4			145.5	0.921	
.5	146.8	0.914	144.6	0.915	

ILLUMINATION UNIFORMITY TEST DATA (Continued)

Distance, Horiz	Intensity, mV	Norm Value	Intensity, mV	Norm Value	5 Mar 76
8.6			142.1	0.899	
.7			139.5	0.883	
.8			137.9	0.873	
.9			137.8	0.872	
9.0	139.9	0.871	138.0	0.873	
9.5	126.4	0.787	–	–	
10.0	117.2	0.729	–	–	

ILLUMINATION UNIFORMITY TEST DATA

EXPANDED SCALE

Position Across Drum, inches	Approx 35-V Input: Relative Intensity Output, millivolts	Approx 35-V Input: Normalized Values	Approx 40-V Input: Relative Intensity Output millivolts	Approx 40-V Input: Normalized Values	Approx 115-V Input: Relative Intensity Output millivolts	Approx 115-V Input: Normalized Values
5.5	81.9	1.062	159.5	1.049	1833	1.076
.6	81.0	1.051	159.5	1.049	1804	1.059
.7	81.7	1.060	159.4	1.048	1814	1.065
.8	80.3	1.041	159.8	1.051	1792	1.052
.9	80.5	1.044	158.0	1.039	1799	1.056
6.0	77.1	1.000	152.1	1.0000	1703	1.000
.1	78.3	1.016	154.1	1.017	1743	1.023
.2	79.2	1.027	157.2	1.034	1751	1.028
.3	78.7	1.021	157.3	1.034	1744	1.024
.4	77.2	1.001	157.7	1.037	1697	0.996
.5	80.2	1.040	156.8	1.031	1777	1.043
.6	74.1	0.961	152.4	1.002	1638	0.962
.7	74.7	0.969	154.6	1.016	1641	0.964
.8	74.6	0.968	157.6	1.036	1655	0.972
.9	75.7	9.982	157.1	1.033	1687	0.991
7.0	73.6	0.955	152.8	1.005	1603	0.941
.1	75.3	0.977	150.7	0.991	1652	0.970
.2	74.7	0.969	152.6	1.003	1651	0.969
.3	75.4	0.978	153.9	1.012	1669	0.980
.4	74.4	0.965	153.6	1.010	1642	0.964
.5	74.6	0.968	150.4	0.989	1637	0.961
.6	74.2	0.965	152.0	0.999	1624	0.954
.7	74.4	0.965	151.1	0.993	1643	0.965
.8	76.6	0.994	154.4	1.015	1699	0.998
.9	76.3	0.990	153.4	1.009	1686	0.990
8.0	74.4	0.965	151.1	0.993	1645	0.966
.1	73.6	0.955	147.6	0.970	1585	0.931
.2			150.3	0.998		

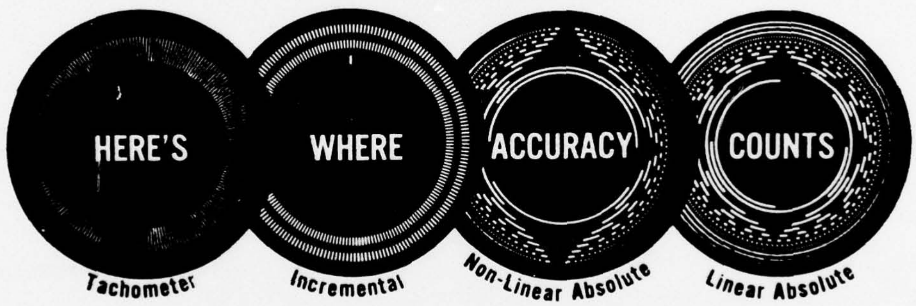
APPENDIX B (TO TR 2020 APPENDIX C):

BALDWIN 5V670 SERIES

OPTICAL INCREMENTAL ENCODERS

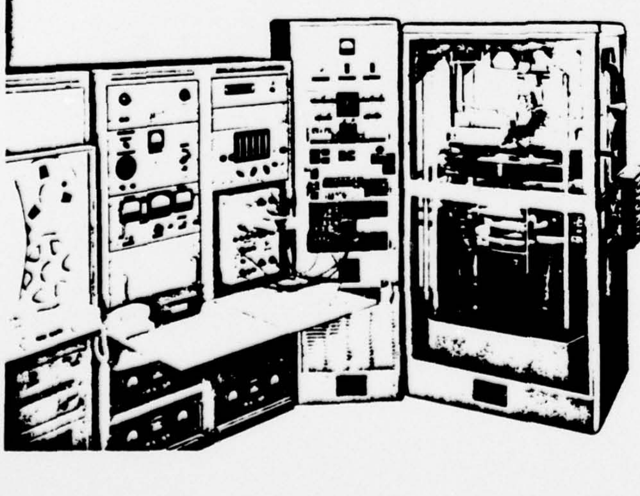
Features

- One input voltage (+5VDC)
- Quadrature and bidirectional pulsed outputs from TTL internal electronics
- Single 100,000 hour light source, field replaceable without calibration
- Resolutions to 48,000
- Solid, hollow or through shaft options



Baldwin Superiority Starts Here

and it's what's inside that counts!



This is the Baldwin Divided Circle Machine, whose output results in the production of the *world's most accurate optical encoders*. There is only one such machine, but there are hundreds of Baldwin Encoder customers who can prove this equation:

BDCM = 0.3 arc seconds

. . . wherein the Baldwin Divided Circle Machine (BDCM) equals centerline-to-centerline accuracies *better than* 0.3 arc seconds of true position!

Glass disks available using photographic emulsion or metallic coatings.

If your specifications and product integrity depend upon the ultimate in *encoder accuracy*, depend on Baldwin. Phone the Baldwin representative nearest you, or contact the general offices.

ELECTRICAL SPECIFICATIONS

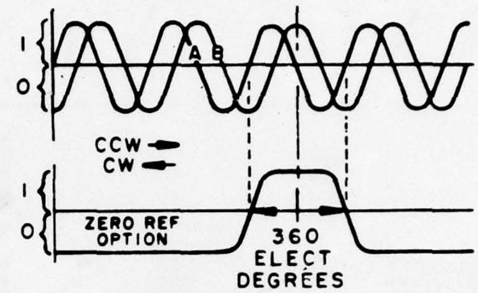
OUTPUT CHARACTERISTICS

Encoders without electronics

Model	Avg. P-P Swing	Avg. Internal Shunt Resistor
5V670	38MV	3.0K
5V671	38MV	3.0K
5V672	38MV	3.3K
5V673	36MV	3.3K
5V674	36MV	3.3K
5V675	35MV	3.3K
5V676	33MV	3.3K
5V677	33MV	3.3K
5V678	31MV	3.3K

The encoders have resistors installed in parallel with the photocell outputs for calibration purposes. For maximum accuracy the outputs should be discriminated at 20MV.

PHOTOCELL OUTPUT WAVEFORMS



Encoders with Electronics Option A or AZ

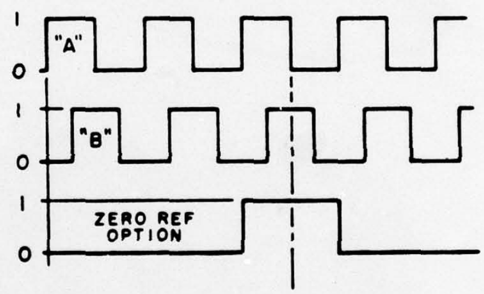
Binary "1"

- Open circuit voltage .. + 3.8VDC ± 0.5VDC
- Output impedance ... 160 ohms, typical
- Risetime and falltime① 200 n sec., maximum

Binary "0"

- Open voltage .... + 0.4VDC, maximum
- Sinking current ...... 16.0ma., maximum

SCHMITT TRIGGER OUTPUT WAVEFORMS



*Encoders with Electronic Option B, BZ, C, CZ, D or DZ*②

Binary "1"

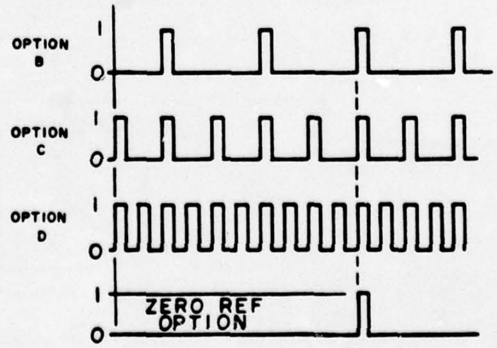
- Open circuit voltage .. +3.8VDC ± 0.5VDC
- Output impedance ... 160 ohms, typical
- Pulse width③ .... 4 μsec., + 1,—2 μsec.
- Risetime and falltime① 200 n.sec., maximum

Binary "0"

- Output voltage .... +0.4VDC., maximum
- Sinking current ...... 16.0ma., maximum

For options B, BZ, C, CZ, D & DZ the count pulses appear on one of two output lines, CW or CCW, depending on direction of shaft rotation.

PULSED OUTPUT WAVEFORMS



① Risetime and falltime measured from 10% to 90% level
② The zero reference pulse occurs coincidentally with a count pulse for logic options only
③ Pulse width measured at the 50% level

FREQUENCY RANGE

OUTPUT FREQUENCY RANGE
Minimum: 0hz all models

OPTIONS

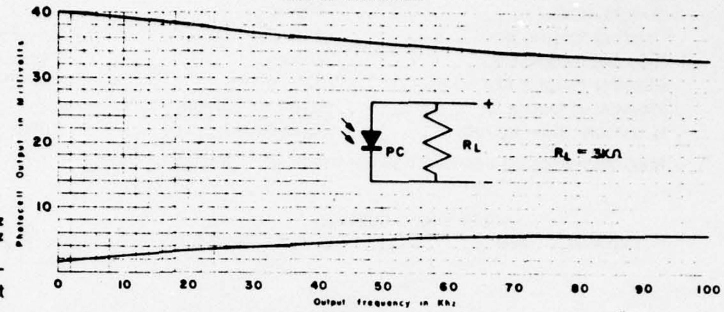
Maximum:**	A&B	C	D
5V670 thru 5V676	50KHz	100KHz	100KHz
5V677 and 5V678	20KHz	40KHz	80KHz

For models without internal electronics operating frequencies at output will be determined by external electronics. Refer to photocell output vs frequency charts for typical curves.

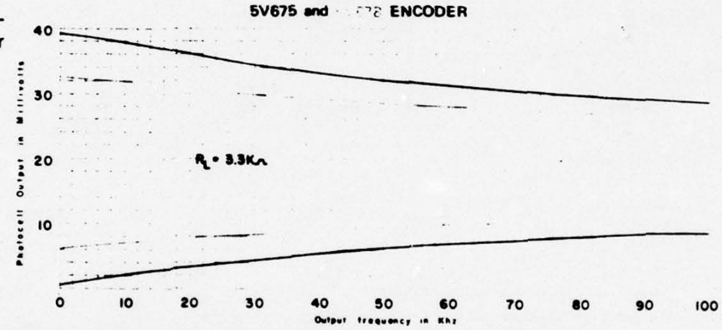
**Higher operating frequencies available upon special order.

AVERAGE PHOTOCELL OUTPUT vs FREQUENCY

5V670 ENCODER



5V675 and [illegible] ENCODER



POWER REQUIREMENTS

Encoders without electronics: 5.0VDC±5% @ 330 ma.

Encoders with electronics

Option	+5.0VDC±5%	Option	+5.0VDC±5%
A	360 ma.	C	385 ma.
AZ	364 ma.	CZ	393 ma.
B	376 ma.	D	385 ma.
BZ	390 ma.	DZ	393 ma.

Power requirements calculated at no load.

Baldwin model P5V power supply is available to supply power for any encoder option.

Baldwin BC 60 counters are complementary units for any encoder with direction sensed options.

ACCURACY

	OPTIONS B	C	D
Bit to Bit RMS(TYP)	2 sec.	13 sec.	15 sec.
Absolute position RMS(TYP)	4 sec.	8 sec.	9 sec.

As resolution increases, RMS error decreases slightly in Option B and significantly more in options C and D.

Accuracy figures were derived from model 5V675 encoders coupled to a Moore divided engine at 21°C.

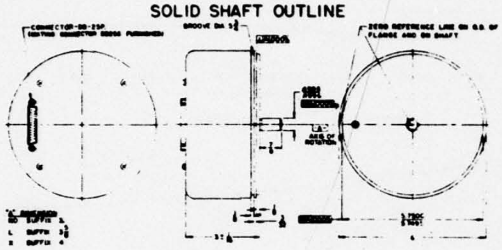
MECHANICAL SPECIFICATIONS

DESIGN FACTORS

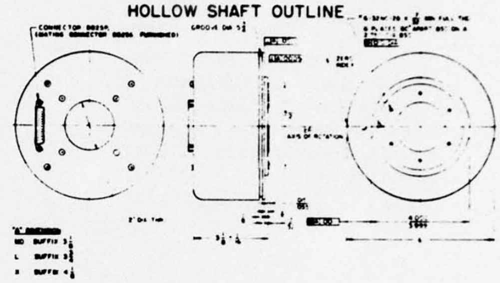
	Solid Shaft	Hollow Shaft	Through Shaft
Weight, max.	4 lb. 8 oz.	5 lb. 7 oz.	4 lb. 14 oz.
Starting torque, max.	3 in.-oz.	6 in.-oz.	3 in.-oz.
Running torque, max.	2 in.-oz.	3 in.-oz.	2 in.-oz.
Bearing fatigue life	50 x 10⁹ rev.	3 x 10⁹ rev.	50 x 10⁹ rev.
Moment of inertia	0.037 oz.-in.-sec.^{2}	0.154 oz.-in.-sec.^{2}	0.0375 oz.-in.-sec.^{2}
Maximum slew speed	15,000 rpm	5,000 rpm	15,000 rpm

Maximum angular acceleration (all models) — 50,000 rad./sec.^{2}

SOLID SHAFT OUTLINE



HOLLOW SHAFT OUTLINE



Working temperature range*:
- Encoder only –40°C to +70°C
- Encoder with electronics 0°C to + 70°C

Storage temperature range:
- Encoder only –65°C to +85°C
- Encoder with electronics –55°C to +85°C

Altitude:
- 70,000 ft., max.

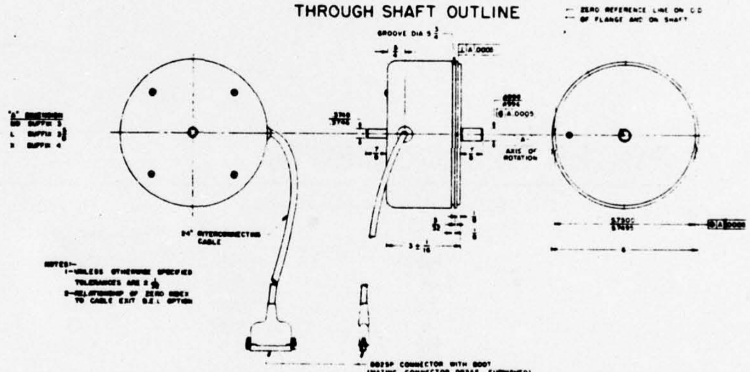
Vibration:
- Meets or exceeds requirements of MIL-E-16400F; MIL-E-5272C.

Shock:
- 50g's @ 11 ms; meets or exceeds requirements of MIL-E-5272C; MIL-E-5400K; MIL-T-5422E

Humidity:
- 98% rh. max. Avoid condensation.

* Wide temperature range models also available on special order.

THROUGH SHAFT OUTLINE



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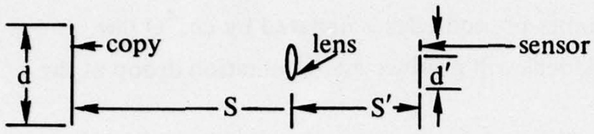
APPENDIX C (TO TR 2020 APPENDIX C):

LENS CALCULATIONS



Ref: TR 1965
P 36-45

d = 8.5 inches

d' = 0.890 inches for Fairchild CCD 121

$$\frac{S}{d} = \frac{S'}{d'}, \text{or } \frac{S}{S'} = \frac{d}{d'} = \frac{8.5''}{0.890''} = 9.550$$

S = 9.550 S'

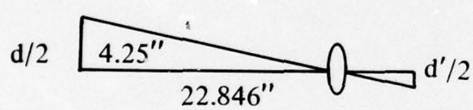
$$\frac{1}{f} = \frac{1}{S} + \frac{1}{S'} = \frac{1}{9.550s'} + \frac{1}{S'} = \frac{10.550}{9.550s'}$$

$$\frac{1}{f} = \frac{1.105}{S'}$$

S' = 1.105f

For f = 55 mm, S' = 60.759 mm = 2.392 (a flat field lens)

S = 22.846 inches



$$\Theta = 90° - \tan^{-1}\frac{22.846}{4.25} = 90° - 79.462° = 10.538°$$

$\cos\Theta = 0.983$

$\cos^4\Theta = 0.9342$

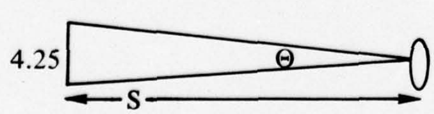
% end intensity = 93.42%

% droop = 6.58% (±3.29%)

For end intensity % $\geqslant \frac{63}{64} = 0.984375 = \cos^4\Theta$

$\cos\Theta = 0.99607$

$\Theta = \cos^{-1} 0.99607 = 5.0809°$



$S = 4.25 \cot\Theta = 47.80$ inches

Then $S' = \frac{47.80}{9.55} = 5.00$ inches

Then $\frac{1}{f} = \frac{1}{S} + \frac{1}{S'} = \frac{1}{47.8} + \frac{1}{5.0} = 0.2207$

f = 4.531 inches = 115.07 mm

Conclusions

1. Uniformity of intensity at scanner photodiodes is dictated by $\cos^4\Theta$ law.

2. Using a Nikon 55-mm flat field lens will produce an illumination droop at the edges of the copy to 93.42% of the center.

3. Conversely, to produce an illumination droop of less than 1/64 (±0.5 lsb for 2^6 gray scale levels), the lens to copy distance, s, must be at least 47.8 inches.

APPENDIX D (TO APPENDIX C):

ABERRATION ERRORS
FOR
CURVED SURFACE TRACKING IMAGING

S = Spacing of pel resolution in inches at object plane
N = Number of pels in the direction of copy motion
E = Error in inches at extreme of object plane
W = Width of copy scanned in inches
R = Radius of transport drum
D = Distance from object plane to lens in inches

Let 2P = true height of copy scanned. Then P = height of true image above drum axis. Assuming a piece of copy having a length 2P is attached to the curved drum, then

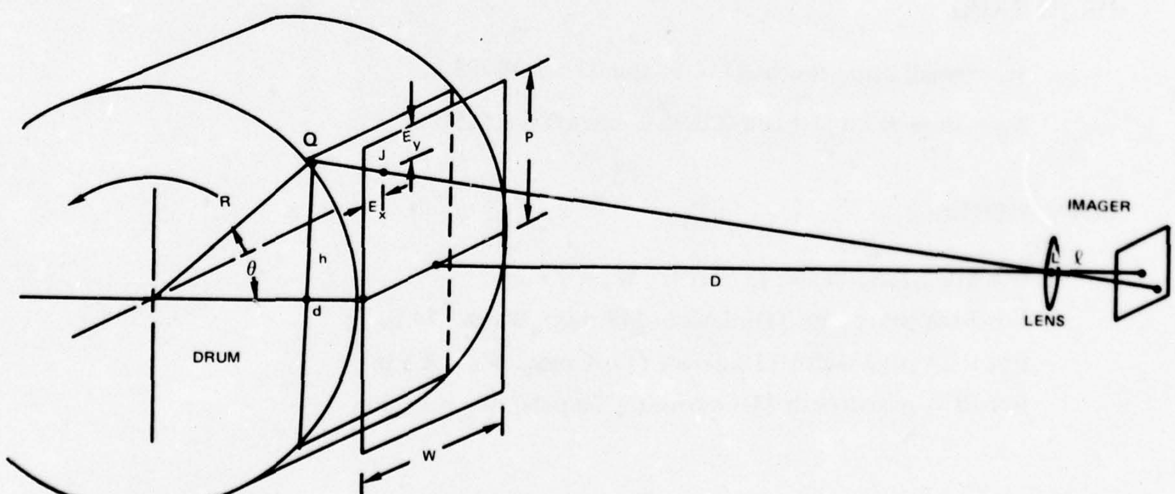
$$P = \frac{2\pi R\Theta}{360^\circ}$$

P also = NS/2

$$h = R \sin \Theta$$

$$d = R - R\cos\Theta = R[1 - \cos\Theta].$$

If the lens is assumed to have X, Y, Z coordinates of 0, 0, 0, then the coordinates of the point Q can be stated



$$X_Q, Y_Q, Z_Q = \frac{W}{2}, R \sin \Theta, R[1 - \cos \Theta] + D.$$

The coordinates of the point J can be found by the intersection of the line QL with the tangent image plane.

$$X_J = X_Q \cdot \frac{D}{Z_Q}$$

$$Y_J = Y_Q \cdot \frac{D}{Z_Q}$$

$$Z_J = Z_Q \cdot \frac{D}{Z_Q} = D$$

$$E_X = \frac{W}{2} - X_J = \frac{W}{2} - \frac{W}{2}\left(\frac{D}{R[1 - \cos \Theta] + D}\right) = \frac{W}{2}\left(1 - \frac{D}{R[1 - \cos \Theta] + D}\right)$$

$$E_Y = P - Y_J = \frac{NS}{2} - \frac{DR \sin \Theta}{R[1 - \cos \Theta] + D}$$

where

$$\Theta = \frac{90 \text{ NS degrees}}{\pi R}$$

For USPS/NELC time delay integration (TDI) experiments the following parameter values are under consideration: Resolution of 200 pels/in only S = 0.005 in. Lens focal length = 55 mm only

DRUM RADII

R_1 = small drum test bed (12-in crcmf) = 1.90985 in

R_2 = large drum test bed (40.96-in crcmf) = 6.5190 in

COPY WIDTHS

For SID 51232 device (320 pels), W_1 = 1.6 in
For RCA prototype TDI device (748 pels), W_2 = 3.74 in
For RCA page width TDI device (1700 pels), W_3 = 8.5 in
For RCA page length TDI device (2200 pels), W_4 = 11.0 in

PEL SIZES

For SID 51232 device, $B_1 = 1.2$ mils

For RCA TDI imagers, $B_2 = 0.6$ mils

NUMBER OF PELS IN DIRECTION OF COPY MOTION

Maximum considered, SID 51232,	$N_1 = 512$
Maximum tested, SID 51232,	$N_2 = 190$
RCA prototype option 1,	$N_3 = 96$
RCA prototype option 2,	$N_4 = 64$
RCA prototype option 3,	$N_5 = 32$

Given a 55-mm lens and a fixed resolution of 200 pels per inch, the distance from lens to drum is dependent on imager resolution only.

CALCULATING FOR USE WITH 1.2-MIL PELS

$$\frac{D_1}{\ell_1} = \frac{S}{B_1} = \frac{0.005}{0.0012}, \text{ or } D_1 = 4.166\ell_1$$

$$\frac{I}{F} = \frac{I}{D_1} + \frac{I}{\ell_1} = \frac{I}{4.116\ell_1} + \frac{I}{\ell_1} = \frac{5.166}{4.166\ell_1}$$

$$\ell_1 = \frac{F\,5.166}{4.166} = 5 \text{ mm} \times \frac{5.166}{4.166} \times \frac{\text{in}}{25.4 \text{ mm}} = 2.6850 \text{ in}$$

$$D_1 = 4.166\ell_1 = 11.1876 \text{ in}$$

CALCULATING FOR USE WITH 0.6-MIL PELS

$$\frac{D_2}{\ell_2} = \frac{S}{B_2} = \frac{0.005}{0.0006}, \text{ or } D_2 = 8.33\ell_1$$

$$\ell_2 = \frac{F\,9.33}{8.33} = 55 \text{ mm} \times \frac{9.33}{8.33} \times \frac{\text{in}}{25.4 \text{ mm}} = 2.42520 \text{ in}$$

$$D_2 = 20.21 \text{ in}$$

SOME DRUM SUBTENDED ANGLES OF SELECTED RADII AND PEL HEIGHTS

For large drum and 510 pels,

$$\Theta_1 = \frac{90 \text{ NS degrees}}{\pi R} = \frac{90 \times 512 \times 0.005 \text{ deg}}{6.519\,\pi} = 11.25 \text{ deg}$$

For large drum and 190 pels,

$$\Theta_2 = \frac{90 \times 0.005}{6.519\,\pi} \times 190 \text{ deg} = 0.0219726 \times 190 \text{ deg} = 4.175 \text{ deg}$$

For large drum and 96 pels, $\Theta_3 = 2.109$ deg

For large drum and 64 pels, $\Theta_4 = 1.406$ deg

For large drum and 32 pels, $\Theta_5 = 0.703$ deg

For small drum and 190 pels,

$$\Theta_4 = \frac{90 \times 0.005}{1.9099\,\pi} \times 190 \text{ deg} = 0.075 \times 190 \text{ deg} = 14.250 \text{ deg}$$

For small drum and 96 pels, $\Theta_5 = 7.2$ deg

For small drum and 64 pels, $\Theta_6 = 4.8$ deg

For small drum and 32 pels, $\Theta_7 = 2.4$ deg

Example 1, using large drum, 512 pels of SID 51232 imager:

$$E_x = \frac{W}{2}\left(1 - \frac{D}{R(1-\cos\Theta) + D}\right) = \frac{1.6 \text{ in}}{2}\left(1 - \frac{11.1876 \text{ in}}{6.519\,[1-0.98078] + 11.1876}\right)$$

$$E_x = 0.00886 \text{ in}$$

$$E_x = \frac{NS}{2} - \frac{DR\sin\Theta}{R[1-\cos\Theta] + D} = 1.28 - \frac{14.22832}{11.31286} = 0.02229 \text{ in}$$

Example 2, using large drum, 190 pels of SID 51232 imager:

$$E_x = \frac{1.6}{2} \text{ in}\left(1 - \frac{11.1876}{6.519\,[1-0.997437] + 11.1876}\right) = 0.0012 \text{ in}$$

$$E_y = 0.48 \text{ in} - \frac{11.1876 \times 6.519 \times 0.0728}{11.2043} = 0.00613 \text{ in}$$

Example 3, using large drum, 96 pels of RCA TDI prototype (748 pels wide):

$$E_x = 1.87 \text{ in}\left(1 - \frac{20.21}{6.519\,[1-0.9993226] + 20.21}\right) = 1.87 \text{ in}\left(1 - \frac{20.21}{20.2144}\right)$$

$$= 0.00041 \text{ in}$$

$$E_y = 0.24 \text{ in} - \left(\frac{20.21 \times 6.519 \times \sin 2.109^\circ}{6.519\,[1-\cos\Theta)] + 20.21}\right) = 0.00149 \text{ in}$$

Example 4, using large drum 64 pels of RCA TDI prototype:

$$E_x = 1.87 \text{ in}\left(1 - \frac{20.21}{6.519\,(1-\cos 1.406^\circ) + 20.21}\right) = 0.00018 \text{ in}$$

$$E_y\ 0.16 \text{ in} - \frac{20.21 \times 6.519 \times \sin 1.4^\circ}{0.0019627 + 20.21} = 0.16 - \frac{3.2327}{20.21196} = 0.00006 \text{ in}$$

Example 5, using large drum, 96 pels of RCA page width imager (1700 pels wide):

$$E_x = 4.25 \text{ in} \left(1 - \frac{20.21}{20.2144}\right) = 0.00093 \text{ in}$$

$$E_y = 0.24 \text{ in} - 0.23851 \text{ in} = 0.00149 \text{ in}$$

Example 6, using small drum test bed, 190 pels of RCA SID 51232 (320 pels wide):

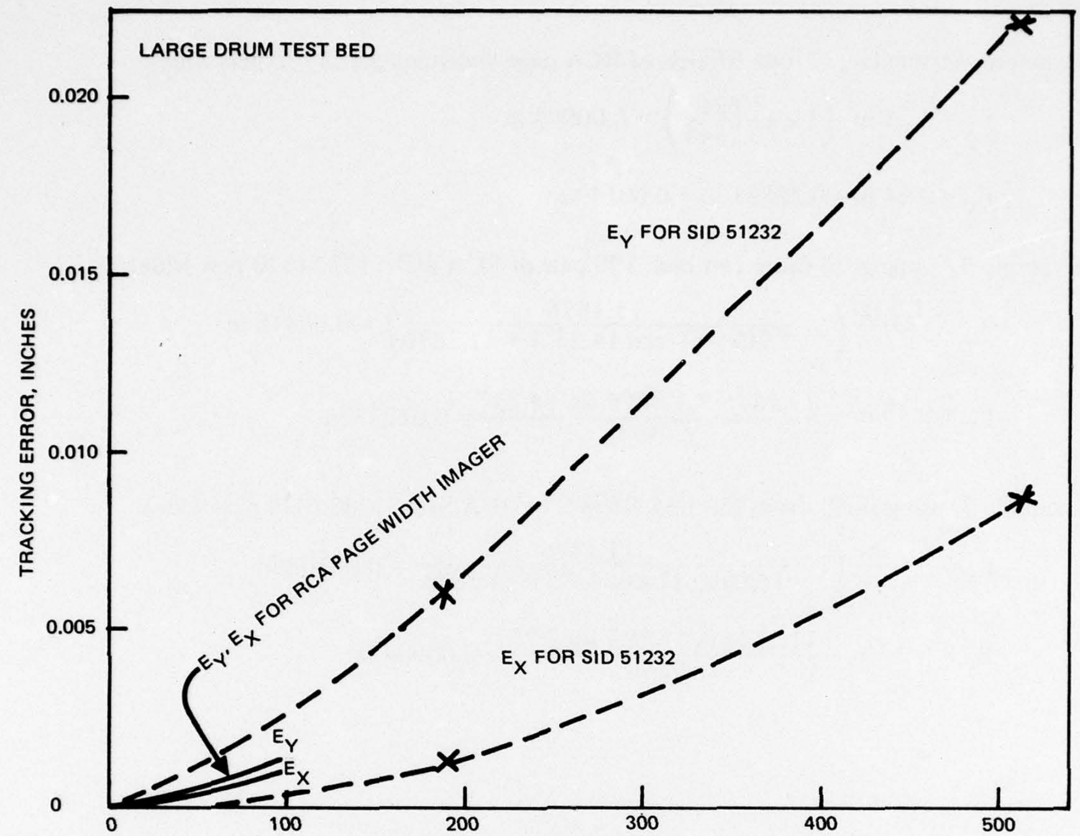
$$E_x = \frac{1.6 \text{ in}}{2} \left(1 - \frac{11.1876}{1.9099\,[1-\cos 14.25°] + 11.1876}\right) = 0.00418 \text{ in}$$

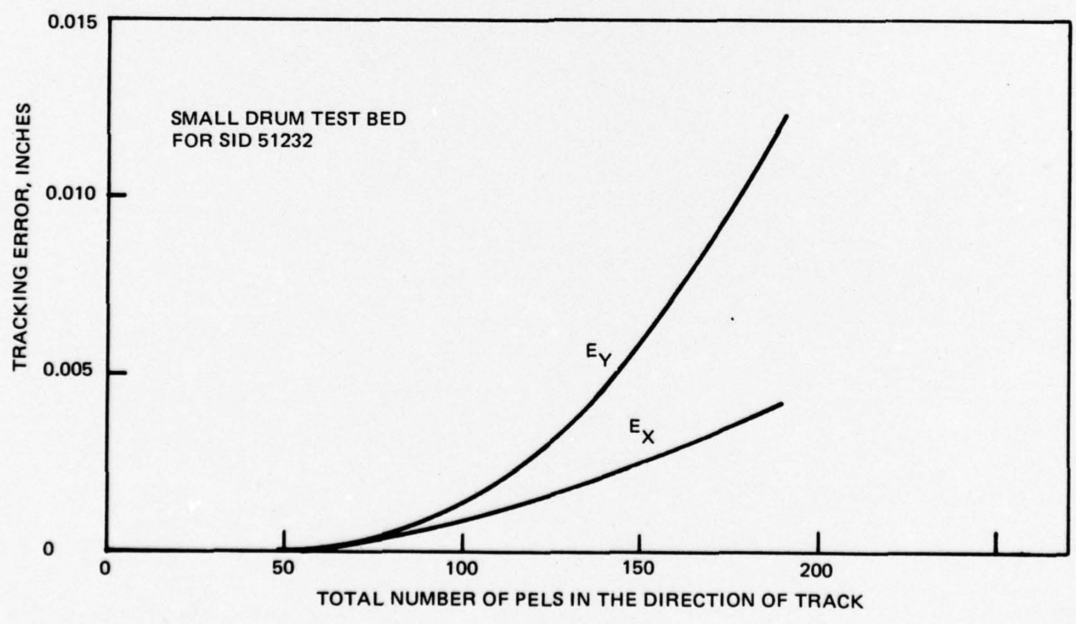
$$E_y = 0.48 \text{ in} - \frac{11.1876 \times 1.9099 \sin 14.25°}{1.24636} = 0.01233 \text{ in}$$

Example 7, using small drum test bed, 96 pels of RCA SID 51232 (320 pels wide):

$$E_x = \frac{1.6 \text{ in}}{2} \left(1 - \frac{11.1876}{1.9099½\,[1-\cos 7.2°] + 11.1876}\right. = 0.00108 \text{ in}$$

$$E_y = 0.24 \text{ in} - \frac{11.1876 \times 1.9099 \sin 7.2°}{11.20266} = 0.00094 \text{ in}$$


LARGE DRUM TEST BED
TRACKING ERROR, INCHES
0.020
0.015
0.010
0.005
0
E_Y FOR SID 51232
E_Y, E_X FOR RCA PAGE WIDTH IMAGER
E_X FOR SID 51232
E_Y
E_X
0
100
200
300
400
500


0.015
SMALL DRUM TEST BED
FOR SID 51232
TRACKING ERROR, INCHES
0.010
0.005
0
E_Y
E_X
0
50
100
150
200
TOTAL NUMBER OF PELS IN THE DIRECTION OF TRACK

APPENDIX D: DATA COMPRESSION

Prepared

for

US POSTAL SERVICE

October 1976

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INTRODUCTION

This project is one of six detailed technical summary reports provided as inputs from NELC to the USPS which discuss specific areas of high importance and interest on the subject of image acquisition. The process of acquiring and analyzing the images used as subjects in this report required the full performance of essentially all the hardware and software resources of the USPS/NELC test bed. We are pleased to add that after the long and painful process of debugging, the entire operation was flawless.

A digitized image contains 3.74 million 6-bit words which are handled and modified dozens of times during acquisition and analysis. Computations can be made on each hard-copy page to show that exactly all the pels are accounted for.

The title of the report indicates that the only use of data acquired is for compression. This is not the case. The data are also useful for the establishment of threshold, choice of illumination color, and gain control of the analog output signal of the imaging device itself. These uses of the data are described in the Prestorage Processing summary report dated May 1976.

Due to the limitations of schedule, the data base of copy materials to be tested during this time frame was somewhat restricted, and a broad statistical basis for our conclusions was not obtained. It is projected, however, that analyses of this type will be continued throughout the remaining year of the program and that a more creditable substantiation of results will be obtained during this period.

RATIONALE FOR COMPRESSION STUDY

Although NELC's purview in image acquisition does not contain a requirement for the development of US Postal Service compression algorithms, there are a number of reasons for which NELC should perform the study described by this report. The team members of NELC Scanner Project have at least an acquaintanceship with the various fixed and variable run length coding (RLC) techniques and also the one- and two-dimensional Hadamard and cosine transform functions investigated by other divisions in NELC. From the imaging data acquired to date there has been no indication as to which of these choices of compression may be more suitable for the Postal Service data transmission system. Perhaps, then, the most important reason for the compression study is to understand the various methods that exist for compression and assure that we do not conceive or recommend a prototype design for USPS scanner terminal equipments which would preclude the use of one or more of the better compression approaches.

A second reason for studying compressibility is the possibility of saving or reducing the quantity of high-speed solid-state storage necessary to contain an entire page of latent image in digital form.

A third reason for studying compression is related to the wide versatility of the test bed itself. The prescanner concept which provides for pel brightness statistics resulting from an image analysis may afford sufficient a priori knowledge of a particular image to allow a choice of compression algorithms to be invoked on a main-scanned image. This would result in considerable savings in frame store page memory as described above. The test bed equipment contained about 95% of the hardware capability to perform the analysis necessary for the study of compressibility of images using run length coding. Only a minor amount of additional hardware was required in order to be able to tabulate the run length coding in both Gray and binary codes in order to document the compressibility of pages of copy of various types.

The fourth reason for the study is to assess the credibility of the claims of many companies in the field of compression offering proposals containing high compression ratios.

The fifth and last reason for the compression study is, of course, the conservation of bandwidth. At 20 pages per second the existing digital image bandwidth required approaches 504 megabits per second. Any modest contribution which may stem from the NELC test bed investigation will be worthwhile in the reduction of this formidable bandwidth requirement.

USPS GENERAL IMAGING REQUIREMENTS

The design goals for USPS image acquisition are exceedingly demanding on scanner and processing electronics technology. These goals are discussed in detail in the First Annual Report for Advanced Mail Systems Scanner Technology, dated 22 October 1975. The desired operating specifications are included here for reference as follows:

Copy rate	Up to 20 sheets per second
Copy size	8½ by 11 inches
Copy velocity	Up to 240 inches per second
Image resolution	200 picture elements (pels) per inch by 200 pels per inch
Images accommodated	Text or continuous tone photographic materials, either black and white or color

The resulting imaging requirement includes the acquisition of 48 000 scan lines per second at about 1700 pels per line; this is a video rate of approximately 84×10^6 pels per second. Dynamic range of the image scanner must be at least 2^6 (or 64) brightness levels.

EXPECTATIONS

Before the data were acquired for the compression study, there were a number of expectations which were predicted to result from the study. These will be listed here but will be discussed as the data are analyzed further in the report. The first expectation was that we would have no difficulty in differentiating most black and white bilevel images from continuous tone images. This is necessary to exploit a strategy that distinctly different compression algorithms may be used for bilevel and continuous tone images. Those used with bilevel, or black and white only, may contain compression ratios which are exceedingly high with respect to those required for continuous tone images.

There was also an expectation that statistical results from "similar" types of images will be in the final analysis somewhat "similar." Although our data base for this report will be extremely small, we hope to prove that, for example, typewritten pages have a particular and identifiable set of statistics and that regardless of contents of a page, size of type, color ribbon, etc, the data will be restricted to a classification which can be recognized by computing techniques.

An obvious expectation is that there will be longer runs of run length coding on the higher-order bit planes. We also expect that the use of Gray code as opposed to binary code may double the length of the runs for a particular image. If this is true, then the number of runs will be divided by two and a 2-to-1 increase in compressibility will be achieved.

In analyzing the data, it is hoped that we can make some recommendations to the USPS as to the most promising compression strategies which they may wish to pursue.

SUBJECTS TESTED

The time to acquire the test data shown in the Test Procedure section is approximately 3.5 hours of test bed time per subject. Therefore, the number of subjects to be tested for inclusion in this report has been somewhat restricted. The following types of documents were used as subjects for this report.

1. IT/8 – Plain white page of typing paper, acquired at a lens opening of f16 with no filter.
   Testing a white page defines the uniformity of reflectance from copy after illumination correction. It also establishes the average brightness compared to the white standard.

2a. IT/3 – Our standard typed page, at f16 with no filter (fig D1).
   The typed page with no filtration gives evidence of change of statistics due to "typical" typed message on the same page stock as analyzed from test 1.

2b. IT/5 – Typed page, at f5.6 with red filter and adjusted illumination.

2c. IT/4 – Typed page, at f5.6 with green filter and adjusted illumination.

2d. IT/6 – Typed page, at f5.6 with blue filter and adjusted illumination.

These tests show any changes in reflectance of paper background and ink (TECH II IBM ribbon) as a function of illumination color.

2e. IT/2 – Typed page, f stop adjusted, no filter, thresholded.

This test will show the results of a fixed selected threshold level on illumination corrected data. The analysis of bit plane 6 will give run length compressibility figures for binary transmission of "typical" typed page.

3. IT/9 – IEEE facsimile chart, at f16 with no filter (fig D2).

The IEEE facsimile chart is widely used and reported on by others. Having statistics will allow comparison with other data bases.

4. IT/11 – Photograph of Ampex plant, at f16 with no filter (fig D3).

5a. IT/7 – Photograph of 40.96-inch Pitney Bowes (PB) drum, at f16 with no filter (fig D4).

5b. IT/13 – Photograph of 40.96-inch Pitney Bowes (PB) drum, f adjusted, dynamic range amplified, no filter.

By readjusting level and f stop, we can expand the contrast to utilize the entire 64 digital brightness levels. The customer may not wish to have the contrast range of his subject matter increased as it is acquired. For this test, an analysis of the appearance of the enhanced results will be meaningful.

6. IT/10 – USPS Headquarters announcement 771, f16 no filter (fig D5).
USPS 771 appears to be a Xerox print. Since it has a heading and logo block, we can tell if it changes the statistics appreciably.

7. IT/12 – Sample of Versatec's electrostatic printer output, printed at a resolution of 200 by 200 dots per inch (fig D6).

22 February 1976

Mr. W. J. Miller, Director
Office of Advanced Mail Systems Development
11711 Parklawn Avenue
Rockville, Maryland 20852

Gentlemen:

This is a sample of the letter we propose to use as a "standard" for imaging experiments at NELC, San Diego. It was made on a Wang System 1222 Dual Cassette Typewriter which consists of a modified IBM Selectric typewriter, two cassette holders, and a magnetic core memory capable of storing pages of data such as this letter. The cassette tapes are being made to store the data for each character in United States of America Standard Code for Information Interchange (USASCII) format. This is a standard seven bit binary code for each character which is widely used in industry. In USASCII form this page as written can be exactly defined by 15099 bits of data (excluding signature, logo or header information). When scanned at 200 x 200 picture elements per inch with six bits per element for grey scale the page is defined by 22,440,000 bits.

By recording the contents of this letter on cassette tape, it is possible to reproduce a quantity of duplicate originals, all nominally exactly the same. Since the typewriter is an IBM Selectric it is also possible to change the type font without changing the message. It is also possible to change ribbons (a five- or ten-minute process) to yield copies of differing colors. It is of course possible to write on all textures, colors and weights of paper with or without letter head. It will also allow copies of this text to be analyzed both with and without signatures of various colors.

This ability to provide complete parameter selection and consistency control for analysis of thresholds, contrasts, color separation, compressability coefficients, and character fonts will be of great benefit in quantifying the requirements of U. S. Postal Service Scanner technology.

Frank Martin
NELC Code 3100
Problem N451

Figure D1. Letter dated 22 Feb 76 to WJ Miller.

Figure D2. IEEE facsimile test chart.

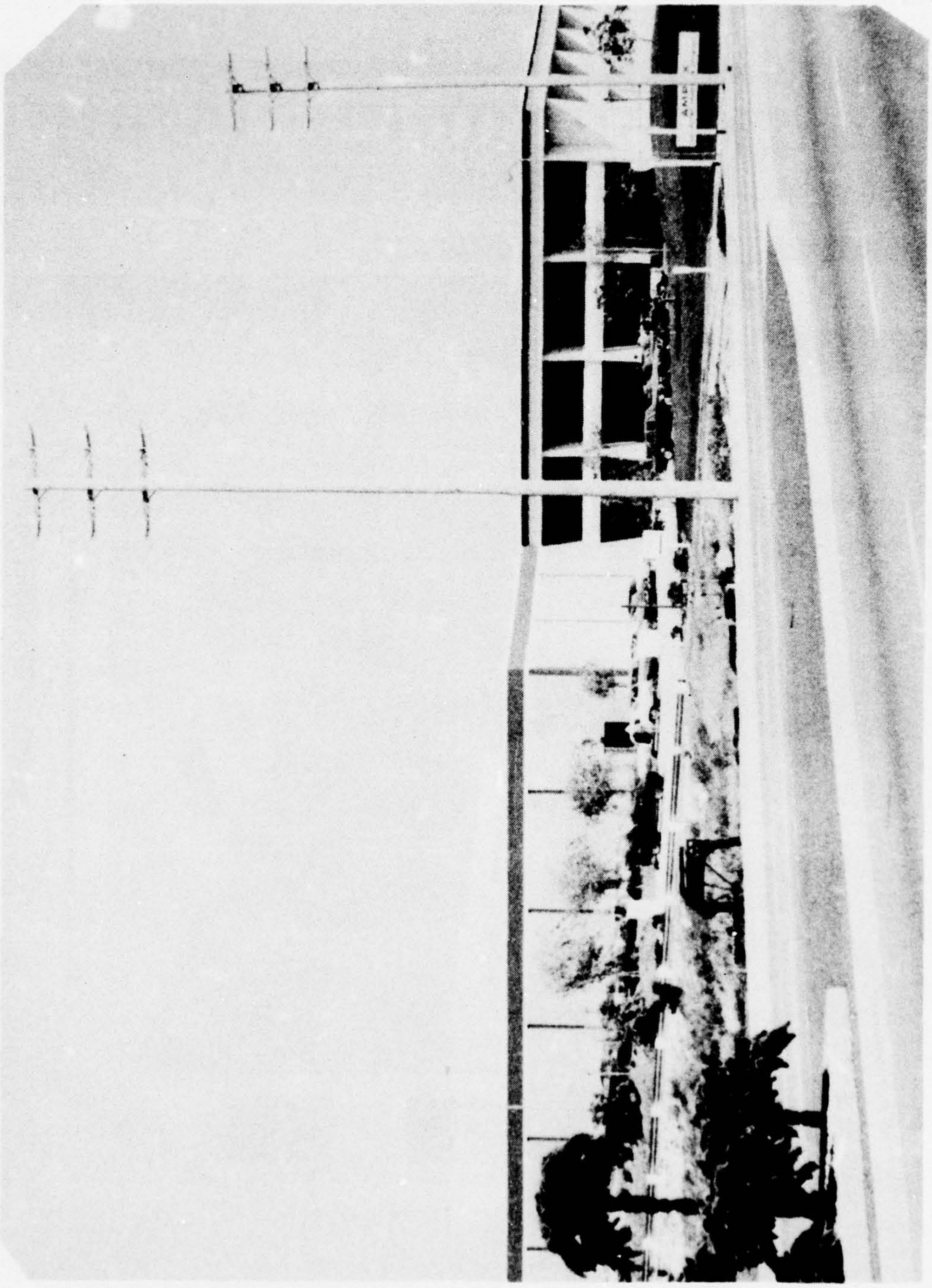

Figure D3. Outdoor photograph.

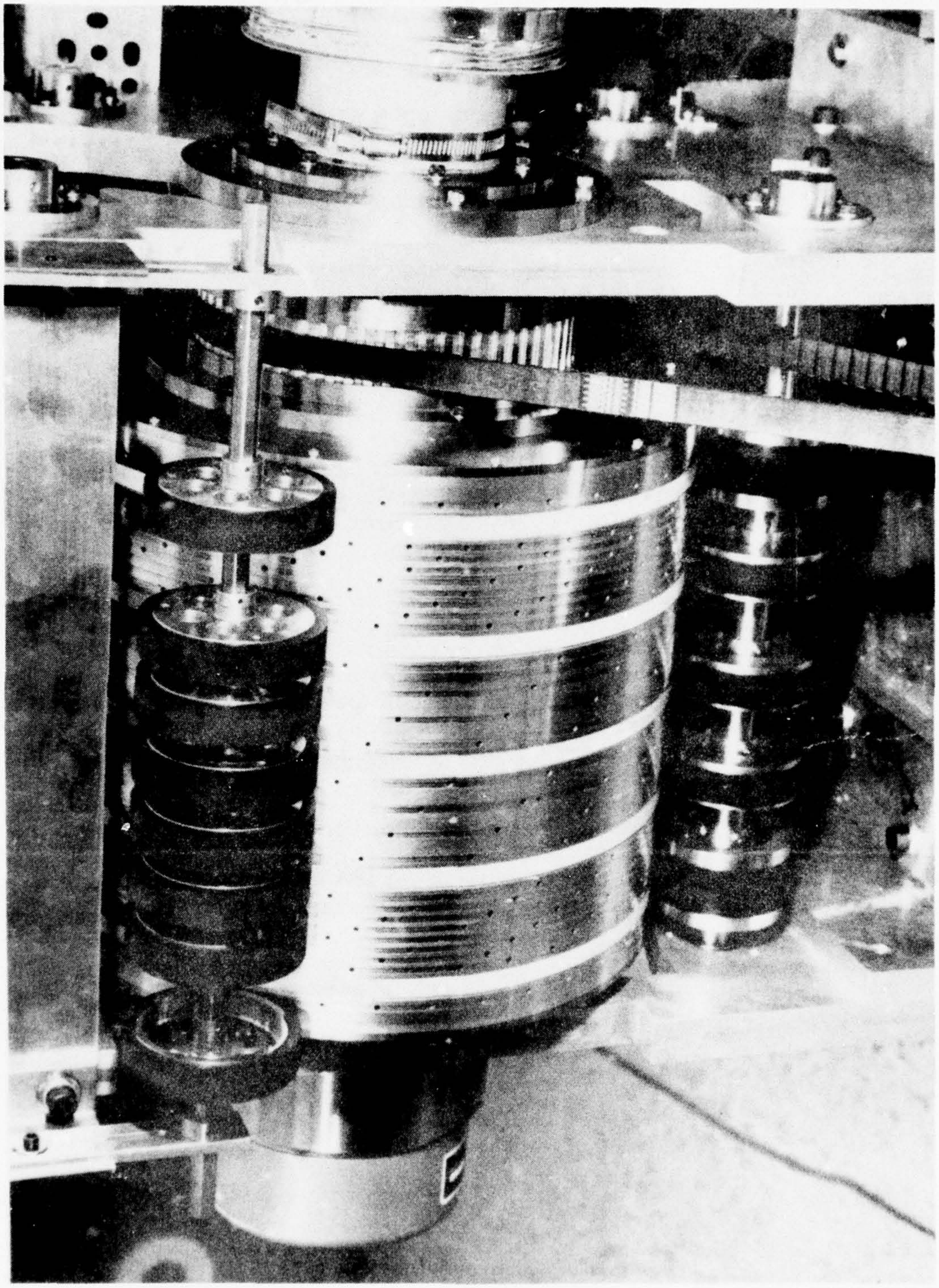

Figure D4. Indoor machinery photograph.

NUMBER: 771	
DATE: 7/23/76	

headquarters announcement

I am pleased to announce the appointment of Joseph F. Morris to the position of Regional Postmaster General for the Western Region effective August 13, 1976, incident to the resignation of William J. Sullivan from that post.

Mr. Morris, a career postal employee of more than 27 years, began his postal service as a substitute city carrier in April of 1949 at the Ardmore, Pennsylvania post office. His service has included numerous supervisory and managerial positions at the local, district and regional levels. Among the positions he has held are foreman, postmaster, postal service officer, regional staff member and is currently the manager of the Delaware Valley District of the Eastern Region.

The selection of Joe Morris to be the Regional Postmaster General for the Western Region is a further continuation of the policy of the U. S. Postal Service to promote qualified career postal employees to the top managerial positions in the Postal Service.

Benjamin F. Bailar

Benjamin F. Bailar
Postmaster General

Figure D5. Headquarters Announcement 771.

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Produce needed documentation. Print timely reports. Plot revealing graphs. Do it all with your minicomputer and mini-matched Versatec printers, plotters, and printer/plotters.
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MINI-PRICED. You can buy a Versatec printer that prints a full 132 columns at 500 lines per minute for less than $5,500. That's $4,000 to $13,000 less than a comparable impact printer. Or if you want printing and plotting, one Versatec printer/plotter replaces a line printer and a pen plotter, saving from $10,000 to $20,000.

MINI-ENVIRONMENTS. More minicomputers are being used in quiet office environments and decentralized installations. Versatec printers use no moving parts in the writing process. They are whisper-quiet and have a MTBF in excess of 3,000 hours.

MINI-CORE. Some plotters demand extensive core. Versatec plotters, using exclusive VERSAPLOT software require only 16 to 32k bytes of core. With a minimum system, you can plot a typical 11 x 8 1/2 plot in a few minutes, and make additional copies in less than 10 seconds each.

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MINI-MATCHED. With the largest product line in electrostatic printing, Versatec has the right machine for your mini and your application.
Find out why Versatec has over 2,000 installed MATRIX units and outsells other electrostatic units two to one.

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The next time your pen plotter runs dry, skips, or smears..
The next time you wait half a day for a complex graph .....
The next time you are down fo repairs.....

Consider the possibility that pen plotters may be obsolete.

Pen plotters are being replaced in many computer plotting applications by Versatec electrostatic plotters and printer/plotters. It's not surprising. Versatec units use no moving parts in the writing process. No moving pens, arms gears, springs, or hammers. Just a quiet hum as plots are produced at up to three inches per second paper speed. This quiet simplicity means lower initial cost and lower operating cost.

But what about software? VERSAPLOT. The world's most powerful raster scan plotting software for electrostatic devices, allows the programmer to construct virtually any graphic representation with a few words of instruction. Subroutine orientation simplifies definition of any graph even those requiring subtle shading. Also, a powerful instructional set and banding technique reduce computer core requirements.

If you want to save existing pen plotter software, our VERSAPLOT II software is a compatible extension that simply adds one subroutine to generate coordinate data and final raster output. Other subroutines and applications require no modification. If you are starting from scratch, our VERSAPLOT I provides a comprehensive easy-to-use FORTRAN subroutine system designed specifically for use with Versatec plotters and printer/plotters. Either way, Versaplot can be used with virtually any computer and for any general plotting application.
Before you ink up your hands with another pen plotter, consider an alternative.

For complete information please write or call:
VERSATEC, INC.
2805 BOWERS AVENUE
SANTA CLARA, CA 95051
(408)988-2800

This sample was produced by a Versatec electrostatic Printer/Plotter. Resolution 200 dots per inch. Dual array writing head. Dot character matrix 16 x 16. Roman Font.

Figure D6. VERSATEC mini-matched printers.

TESTS TO BE MADE

For the subjects to be tested, three types of statistics will be taken – pel brightness, first derivative, and run length statistics. The pel brightness statistics give the distribution of the intensity levels occurring in an image; that is, what portion of the area of an image is black or gray or white. More specifically, totals are accumulated on the number of occurrences of pels at each of the 64 possible brightness levels, throughout an entire image. The brightness statistics may then be displayed in histogram form, an example of which is shown in figure D7. This figure is representative of data obtained from a typewritten page. The large accumulation of pels occurring at high brightness levels corresponds to the background of the typewritten page. The smaller accumulation of pels occurring at lower brightness levels represents that area of the page covered by typewritten characters. The ratio of these two areas of the curve is a direct relationship to the actual print density on the page.

The first derivative statistics represent the magnitudes of changes in the brightness information along each scanned line of an image. To accumulate these statistics, the absolute value of the difference between two successive pel amplitudes is accumulated for each pel in an image, as in figure D8. This information is displayed in histogram form as shown in figure D9. In this figure the number of occurrences is plotted for each of the 64 possible differences between two successive pels. The lower portion of the curve corresponds to relatively slow-changing image information and the upper portion of this curve represents the magnitude of the first pel on each line, since the first difference on a line is taken as the difference between 0 and the first brightness level.

In the third type of statistics, run length statistics, the numbers of runs of lengths 1 through 64 are accumulated. To illustrate the method used, refer to figures D10 and D11. Figure D10 shows typical pel values for a portion of an image line and how the bit planes are organized. Since run length coding may be performed only on a single bit stream, a particular bit plane must be selected at a given time. In this example, bit plane 4 has been selected for analysis.

Figure D11 shows the accumulation of runs of zeros and runs of ones. The NELC digital image analyzer is designed to accumulate statistics on runs of zeros and ones independently, since certain coding schemes operate differently on each. Thus, for a given bit plane and a given polarity of image data, the total numbers of runs of lengths 1 through 64 are counted for the entire image. In the example of figure D11 bit plane 4 has been selected and runs of both polarities are shown. For runs of zeros there would be an increment in the number of runs of length 2 and the number of runs of length 3. For runs of ones there would be one run of 4 counted.

The general characteristics of the run length statistics expected are that the low-order bit planes will have many short runs and few long ones. The higher-order bit planes would then exhibit just the opposite characteristics. Also, the run length statistics will be accumulated on the image data when the binary data are converted to Gray code. The Gray code exhibits the desirable characteristic that there are only about half the number of transitions (hence, run lengths) within all but the most significant bit planes. This should give a significant improvement in the compression of images using run length coding. A comparison of the two codes is shown in table D1.

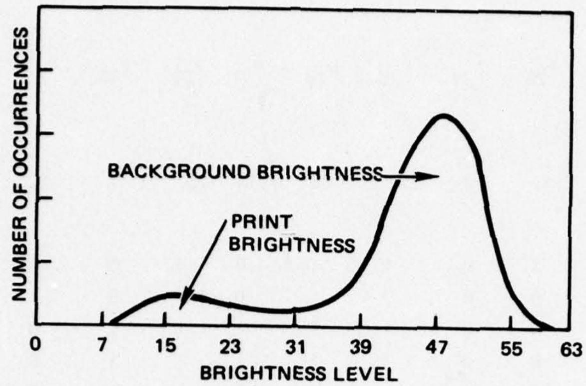

Figure D7. PEL brightness statistics.

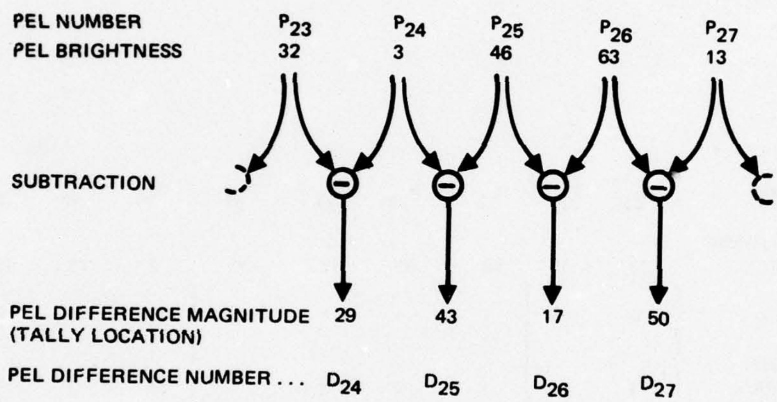

Figure D8. First derivative statistics (1).

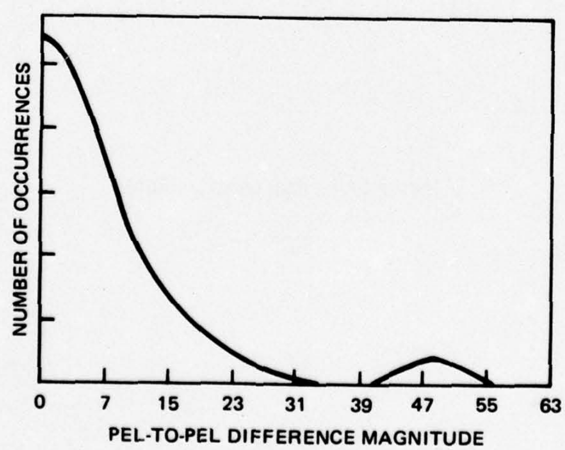

Figure D9. First derivative statistics (2).

		P_{23}	P_{24}	P_{25}	P_{26}	P_{27}	P_{28}	P_{29}	P_{30}	P_{31}	
PEL NUMBER		P_{23}	P_{24}	P_{25}	P_{26}	P_{27}	P_{28}	P_{29}	P_{30}	P_{31}	
PEL BRIGHTNESS VALUE											
DECIMAL		32	3	46	63	13	30	7	16	53	
BINARY											
BIT PLANE	6 MSB	1	0	1	1	0	0	0	0	1	TO RUN LENGTH COUNTER
	5	0	0	0	1	0	1	0	1	1	
	4	0	0	1	1	1	1	0	0	0	
	3	0	0	1	1	1	1	1	0	1	
	2	0	1	1	1	0	1	1	0	0	BIT PLANE SELECTOR
	1 LSB	0	1	0	1	1	0	1	0	1	

Figure D10. Bit plane selection.

PEL NUMBER	P_{23}	P_{24}	P_{25}	P_{26}	P_{27}	P_{28}	P_{29}	P_{30}	P_{31}	
PEL BRIGHTNESS DECIMAL	32	3	46	63	13	30	7	16	53	
BIT PLANE 4	0	0	1	1	1	1	0	0	0	
RUN LENGTH COUNTER	1	2	1	2	3	4	1	2	3	
RUN LENGTH BLACK - 0's		2							3	TALLY LOCATIONS
RUN LENGTH WHITE - 1's						4				TALLY LOCATIONS

Figure D11. Run length counter.

TABLE D1. CODE COMPARISON.

	Binary Code					Gray Code			
	D_1	D_2	D_3	D_4		G_1	G_2	G_3	G_4
	1	1	1	1	WHITE	1	1	1	1
	1	1	1	0		1	1	1	0
	1	1	0	1		1	1	0	0
	1	1	0	0		1	1	0	1
	1	0	1	1		1	0	0	1
	1	0	1	0		1	0	0	0
	1	0	0	1		1	0	1	0
	1	0	0	0		1	0	1	1
	0	1	1	1		0	0	1	1
	0	1	1	0		0	0	1	0
	0	1	0	1		0	0	0	0
	0	1	0	0		0	0	0	1
	0	0	1	1		0	1	0	1
	0	0	1	0		0	1	0	0
	0	0	0	1		0	1	1	0
	0	0	0	0	BLACK	0	1	1	1
Number of Transitions	1	3	7	15		1	2	4	8

TEST BED CONFIGURATION

A block diagram of the NELC image scanning test bed is given in figure D12. A complete description of the large drum scanner test bed is given in the Advanced Imager summary report, with the exception of the analog preprocessing and digital preprocessing sections, which will be added to the system at a later date. A brief description, however, will be given here.

The illumination source is two 18-inch fluorescent lamps with a special blend of red, green, and blue phosphors in ratio of one, two, and eight, respectively. This ratio when combined with the silicon response of the CCD imager will produce nominally flat response throughout the spectrum. Figure D13 shows a plot of the illumination spectral response along with that of the silicon imager.

The paper transport drum consists of a hollow aluminum drum with a circumference of 40.96 inches and a length of 8-3/4 inches. The circumference of the drum was chosen to give exactly 0.005 inch of surface movement per pulse output of a Baldwin shaft encoder. The shaft encoder provides a total of 8192 pulses per revolution of the drum. This is used for synchronizing the scanner with the paper movement.

The imager used for these tests is a Fairchild CCD-121 with 1728 elements organized as a linear self-scanned array. The lens used for imaging is a Micro Auto Nikkor 55-mm f3.5 lens. It is specially designed for flat field imaging applications.

The output from the imager is amplified and input to a sample-and-hold unit, and then to a 6-bit analog-to-digital (A/D) converter capable of 10-megahertz operation. The output from the A/D converter is then input simultaneously to both the digital image analyzer and the memory controller.

The memory controller is a general-purpose processor with special consideration given to image processing. Two levels of control are available through a microprogrammed firmware implementation of hardware function and a simplified machine language instruction set. A complete description of the memory controller is presented in the Frame Store Memory and Display report, dated May 1976. The memory controller is used in several ways in this system. To test high-speed image acquisition, the memory controller acts as a data formatter, packing 6-bit picture elements into 48-bit words for storage in the frame store memory. For image analysis the memory controller is used to store image data on one of the magnetic tape units. The memory controller then reads image information from tape and inputs it to the digital image analyzer for analysis. Once the analysis is complete, the memory controller reads the statistics information from the analyzer and formats it for display on either the CRT monitor or the CRT terminal.

The frame store memory as it now exists is large enough to hold one-eighth of an 8½-by-11-inch image. It is organized as 65k words by 48 bits wide. The cycle time on the memory is 650 nanoseconds, allowing a pel input rate of a maximum 10.5 megapels per second, which is the required data rate for eight such memory modules to capture image information at a 20-page-per-second input rate.

There are currently two magnetic tape units associated with the test bed. There is presently one magnetic tape unit associated with the magnetic tape formatter. This tape unit has a nine-track 1600-bit-per-inch format with a second tape unit to be installed at a later date. The third magnetic tape unit shown in the diagram is a nine-track 800-bit-per-inch tape deck which will be removed from the system when the new magnetic tape unit is installed.

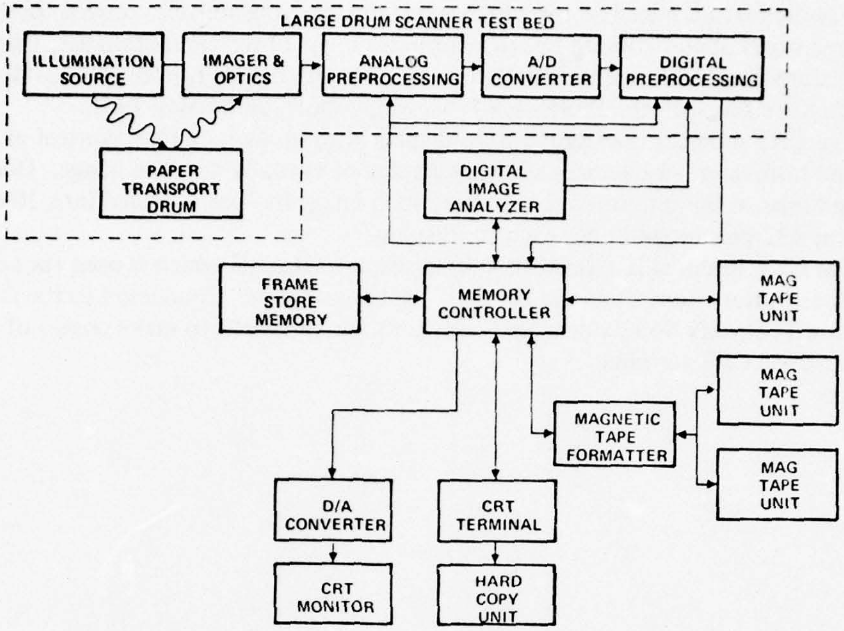

Figure D12. Image scanning test bed, block diagram.

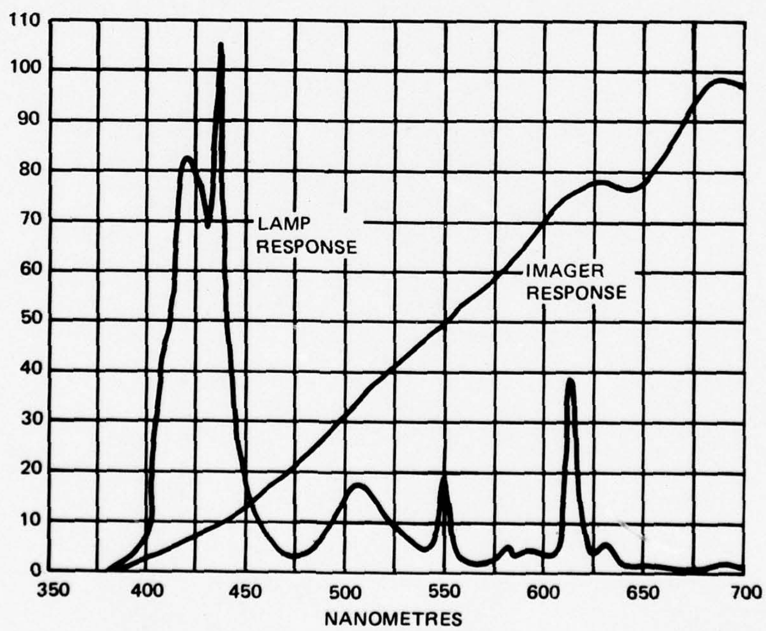

Figure D13. Spectral response.

The digital image analyzer is a high-speed device using emitter coupled logic to gather three types of statistics on image information – pel brightness statistics, first derivative statistics, and run length statistics. A complete description of the digital image analyzer may be found in the Prestorage Processing report, dated May 1976.

The CRT monitor is a Conrac RQB display with phase lock loop control of both vertical and horizontal sweep rates allowing display of virtually any size image. Due to the resolution limits of the monitor the 8½-by-11-inch image has been divided into 20 equal segments of 432 pels by 440 lines each for display.

The CRT terminal is a Tektronix 4023 display terminal which is used for command entry to the memory controller and for data display purposes. Connected to the CRT terminal is a Tektronix 4632 video hard-copy unit which is used to make copies of data displayed on the CRT terminal.

TEST PROCEDURE

The analyses which were run for the computation of data for the compressibility study required a large investment in manpower and machine time. Therefore, it was necessary to ensure that the equipment was in perfect working order. It was also necessary that a repetitive acquisition sequence be followed for the procedure to ensure that all data could be taken under uniform conditions and that the resulting data could be properly identified. This section of the report describes the tests to ensure that the equipment was functioning properly. It also describes the check points in the procedure which assist in the monitoring of the acquisition, analysis, and recording of data.

EQUIPMENT VALIDATION

The first concern in acquiring the data is to validate that the equipment is in proper working order and that meaningful and repeatable results can be obtained reliably. The validation of the equipment status is made by two types of tests using ramp input signals in the scanner equipment.

The first ramp test is done with an analog triangular waveform which is substituted for the output data from the charge coupled device. Figure D14 shows the setup for sampling this analog signal. A function generator module was fabricated and mounted in the module enclosure on the large drum test bed. This circuit produces a triangular waveform having an amplitude from 0 to −2.56 volts. The upper and lower excursions of the waveform (and thereby the amplitude) are adjustable, as is the frequency for establishing the limits of the excursion compatible with the input to the sample-and-hold and analog-to-digital converter. The frequency of the sawtooth ramp does not appreciably affect this experimental result, but it was set in this instance at about 1.25 kilohertz. The ramp sweep is allowed to run asynchronously with respect to the line sampling frequency, which in this series of tests is approximately 9.2 lines per second. The probability of sampling each of the sample levels from 00 to 63 should be equally likely since excursions of the sawtooth ramp signals are quite linear in both positive and negative slopes.

The data from the A/D converter are fed through the image analyzer, which provides a count of the number of times the A/D converter produces any and all of 64 different binary output states. For this test the system is controlled to acquire a set of samples equivalent to 2200 lines of 1700 samples (8½-by-11-inch page at 200 by 200 pels per inch), or a total of 3.74 million samples.

When the counting process in the analyzer is completed, the results are sent to the frame store memory controller, where the 24-bit binary numbers are converted to decimal equivalents and displayed on the CRT terminal. A hard-copy print can then be made of the tabular results. Table D2 is an output showing the results of this test. It can be seen that the number of samples whose values were at level 00 through level 63 was approximately the same. The values of the count in bin 01 and 02 are slightly different from the others, probably due to the proximity of the end points of the ramp. Values in the remaining level bins range from 64 972 in bit 04 to 34 702 in bin 15.

The frame store memory controller also converts the 24 bits of count data from the image analyzer into bar graph lengths for presentation on the Conrac monitor in high-resolution horizontal histogram form and on the Tektronix keyboard and display terminal in low-resolution vertical histogram form. A copy of the low-resolution histogram is shown in figure D15.

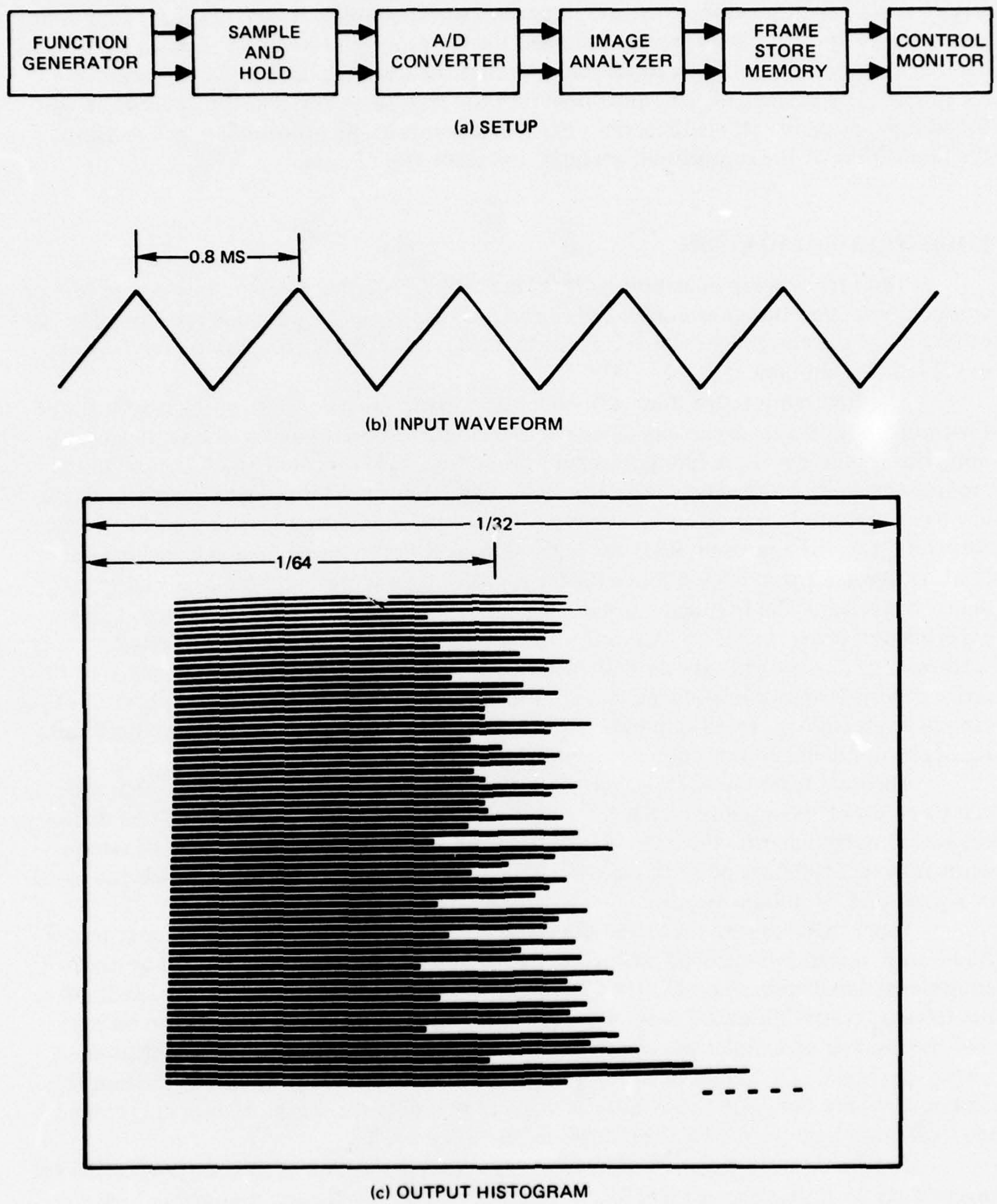

Figure D14. Built-in test mode.

TABLE D2. TEST RESULTS.

0	55154	16	57203	32	56810	48	43954
1	80572	17	48753	33	41485	49	47101
2	72520	18	56096	34	54631	50	54179
3	44132	19	38596	35	44330	51	49271
4	64972	20	52164	36	43777	52	39270
5	58229	21	53842	37	52925	53	53030
6	62117	22	57663	38	56471	54	55974
7	35513	23	37060	39	43974	55	49020
8	60220	24	50560	40	42143	56	37858
9	55566	25	52811	41	52164	57	52537
10	57794	26	55104	42	54390	58	55064
11	37580	27	41780	43	46251	59	54997
12	57175	28	46948	44	41732	60	36397
13	54939	29	53250	45	52849	61	58645
14	61230	30	61476	46	58662	62	55882
15	34702	31	36599	47	43733	63	56358

A/D CALIBRATION TEST   20 SEPTEMBER 76

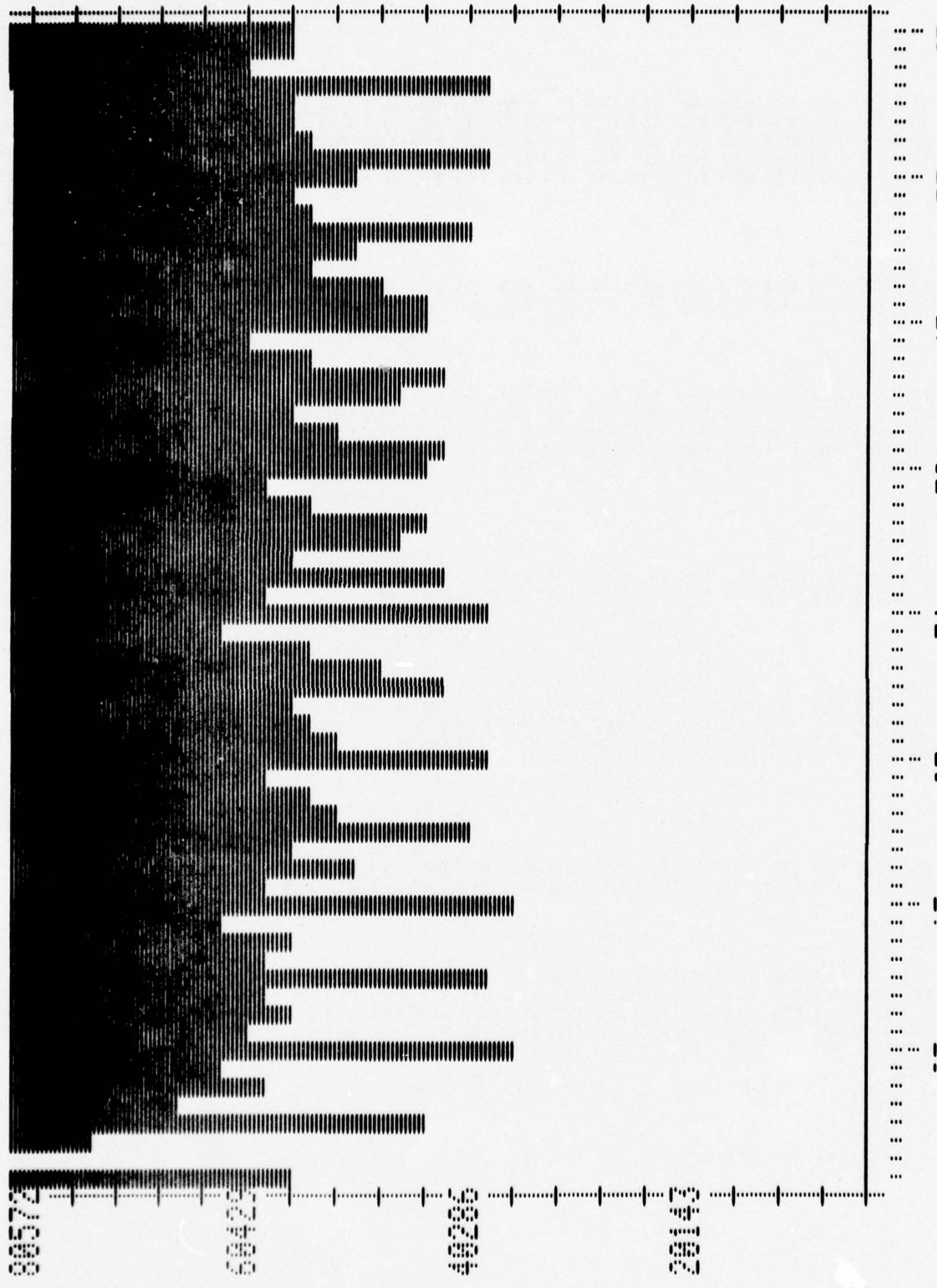

Figure D15. Low-resolution test histogram.

The software program provides magnification or normalization of the image to present the longest high-resolution bar graph display possible on the Conrac monitor without clipping off meaningful data. A copy of a sample histogram corresponding to the data in table D2 is shown in figure D14(c). This is done by testing the data for lack of overflow as the magnitudes of the displayed bar lengths are successively multiplied by values of 2. Six different display magnifications can be presented: 2X, 4X, 8X, 16X, and 32X. To indicate which of these scales is being used for the display, a series of dashes is added to the lower right side of the display. No dash represents no magnification; one dash indicates that the scale is 2X and that all values indicated by bar graph should be multiplied by 2^{-1}. Two dashes indicate that all data should be multiplied by 2^{-2} and so forth, up to five dashes, which indicates that a factor of 2^{-5} should be used. On this latter scale a bar having full screen width represents a quantity of 1/32 of the total count accepted.

The bar graph is the sequence of black lines in the white field which extends from left to right in the photograph. The space for bin 00 is at the bottom and 63 is at the top. Bin 00 represents the blackest signal which can be obtained from the picture and bin 63 the brightest or whitest. A perfect calibration would show all bars having exactly the same length and essentially equal count in all bins in the data of the table. The fact that they are not all equal indicates that there are differences in the uniformity of threshold level of the A/D converter.

It should be noted here that the test bed contains a modest amount of built-in test equipment (BITE) which can in a few seconds verify the proper operation of all the above process following the output of the A/D converter. This is accomplished by providing a simple binary 6-bit counter whose outputs are substituted for the A/D converter output in the test mode. The counter is incremented after each sample so that exactly the same number of counts is sent to the analyzer for each of the 64 possible values if the sequence is stopped in multiples of counts divisible by 64.

A Xerox copy of the Polaroid photograph of the resulting display from a previous test using a different and perhaps more linear external ramp is shown in figure D16.

In our case we use 27 such sequences of 64 per line, which results in a total of 1728 bits per line. (Our program is alterable to allow or prohibit this test to continue beyond the 1700 pels which are taken in a normal image acquisition.) This BITE test has been run many times, and the result verifies that all counts in the analyzer are of equal value and all bars in the display are of equal length. It also verifies that the total number of pels acquired equals 3.74 million. By performing the above two tests, which require data both before and after the A/D converter, and completing the process of data acquisition, storage, analysis, and output presentation, we can validate whether or not the equipment is functioning in a proper and repetitive manner.

Analysis of the data and examination of the bar graph demonstrate in a striking manner the cyclic nature of the residual error of the A/D converter. Near the bottom of the display every fourth bin is longer than the other three. In the center, the uniformity of counts in the bins seems to improve. Near the top, the problem worsens again, but the long bar bin numbers are not now divisible by four. At the bottom they are 04, 08, 12, etc, and at the top they are 63, 59, 55, 51, 47, etc.

The analog-to-digital (A/D) converter used to digitize these 4 data is a two-stage, 6-bit device. The first 4 bits are obtained from the first stage and the least two are obtained from the second. Although some adjustments are available to establish the gain and level of the residue from the first 4-bit conversion for the last 2-bit conversion, the converter

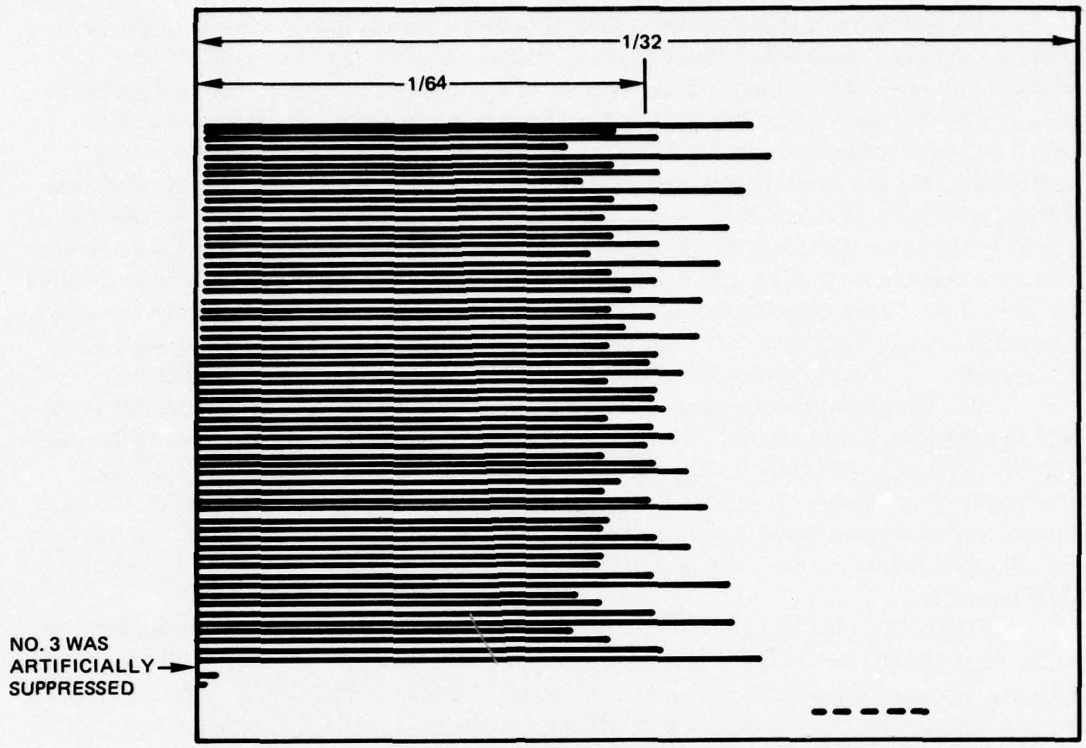

Figure D16. High-resolution test histogram.

appears to have insufficient internal stability to maintain a more exact and uniform relationship for any appreciable period of time. Consequently, cyclic changes in length of the histogram bars can be seen in figure D16.

An analysis of the fine structure in figure D16 indicates the following:

1. The length of the shortest bar (above 04) is 2.0625 inches.
2. The length of the longest bar is 3.125 inches.
3. The length of a "standard" bar is about 2.59 inches.
4. The length of a "standard" bar represents only 1/64 of the total count, or 1.5625%.
5. The total deviation is

$$\frac{3.125. - 2.0625}{2.59} \times 1.5625\% = 0.64\% \ .$$

6. The deviation of ±0.32% is more than two to one better than the specified accuracy of the converter, which is ±0.78125%.

Although the instrumentation has not been designed to perform with more accuracy than ±0.78%, or one part in 64, the appearance of the bar graph histogram is distracting if not misleading. There are three alternatives to the problem. The first is to try to procure an A/D converter of sufficiently high accuracy so that the unevenness in the distribution

does not noticeably exist. This may require a 10- or 12-bit very-high-speed converter which is either nonexistent or very expensive.

The second is to leave the hardware and software unchanged and compensate for the unevenness in the interpretation of the results.

The third is to use a software normalization routine which will utilize the calibration data and multiply each bin content by an appropriate factor to force the corrected calibration bins to be equal at 1/64 of full scale. It is felt that this is the best approach for removing the first-order effects of the nonuniformity for pel brightness statistics. There can be higher-order errors generated by this process. For example, if illumination corrected data provided a majority of two brightness level outputs, one of which fell exactly in the center of one high bin, say 56, and the other exactly in the center of a low bin, say 09, then any multiplication by correction factors would lead to errors in the ratios of the resulting pairs. It is felt that cases of this kind will be infrequent and that for data having statistical characteristics such as we expect from image acquisition, the normalization is a meaningful procedure.

The above two tests indicate that the A/D converter is operating within its specified accuracy. For the time being no correction is being made to the A/D converter output data. During the coming year, a decision will be made whether a higher-performance A/D converter or more sophisticated software is necessary to resolve fine detail in the analysis. The validation process tests the operation of the entire test bed with the exception of the imager and its preamplifier. This includes all modes of the analyzer, two tape decks, controller, software, and hard-copy printer. When all this is seen to operate properly, it is possible to calibrate the illumination levels.

CALIBRATION

The first test to be made in the calibration procedure is to check the response from the A/D converter with the white and the black standards placed in the optical path of the imager.

The white standard is obtained by painting Eastman white reflectance standard (catalog 6091) on a curved metallic plate which can be rotated in front of the illuminated area on the drum. The white reflectance standard is specially purified barium sulfate, which gives a very fine diffuse reflectance of radiant energy from about 200 nanometres in the ultraviolet region to about 2500 nanometres in the near infrared region. The black standard is a black felt material approximately 1 inch wide and extending across the entire drum width. This material, which is obtained from Edmond Scientific Co, provides less reflectance than any other convenient material we have yet measured.

With the white standard in place, the imager amplifier is adjusted in gain and level to provide a digital output of binary 63. Another adjustment is used to produce a binary 00 output from the A/D converter when the black standard is scanned.

It should be noted here that these calibration tests are made with the two broad-spectrum fluorescent lamps at their nominal operating voltage and that no filters are placed over the lens so that the data represent the black and white response of the system. For these tests an f3.5 Micro Auto Nikkor P55-mm lens is used for the acquisition. For the extremes of illumination presented by the white standard and the black felt black standard, the lens is set at f16. The lens is stopped down to this extent at this stage of the calibration so that full response can be given when any of the three color separation filters are used or

when copy samples of low reflectance are used in the analysis process. In these cases the lens aperture can be opened to as much as the full aperture of f3.5 without serious degradation of image quality.

IMAGE ACQUISITION RATE

The image acquisition for these tests is made with the Fairchild CCD-121, which is a 1728-pel device having a maximum output frequency of 1.0 megahertz.

Because of the limited capacity of our solid-state memory, it is necessary to store the complete page images onto nine-track magnetic tapes mounted on the Kennedy tape deck. The storage input rate onto the Kennedy tape seriously slows the system acquisition rate even though it is running at 1600 bytes per inch and 45 inches per second. The tape storage of the data cannot be exactly synchronized with respect to the line advance signal which is received from the Baldwin encoder mounted on the scanning drum. The 0.005-inch incremental signal supplied by the Baldwin encoder must occur with a frequency which is equal to or less than the input line rate of data onto the magnetic tape.

Therefore, the data for full-page images are taken very slowly. It was decided that for this portion of the evaluation, it would be undesirable to change imager clock frequencies, imager integration time, or drum speed. The only variable which was allowed was the f stop on the lens. From preliminary tests, it was determined that the response of the imager when used with any of the three filters was approximately 25% of the output obtained with broadband illumination. Thus, an allowance in initial lens setting of two f stops was required. In order to accommodate low-reflectance materials with a filter, a latitude of two more f stops was desirable.

Our lens is an f3.5 55-mm *Micro* Auto Nikkor. If we chose f4 for low-reflectance tests with filters, then normal reflectance with filters will be accommodated at f8, and f16 will accommodate normal reflectance with no filters. The stop at f16 will also be used for calibrating the system with the white standard. We tried to maintain a constant illumination level for all tests. This was found to be undesirable from the standpoint of fine adjustment and the restriction was dropped.

Once the stop at f16 is chosen, the integration time for acquiring a maximum brightness reflection from the white standard can be chosen. The integration time must be set so that the imager output voltage remains slightly below saturation when viewing the standard.

The CCD121 imaging device has no control to inhibit integration during the exposure period. The 0.005-inch marks from the Baldwin encoder cannot be used because their time periods vary about ±25%. This would cause an erroneous interpretation of image brightness if this variation were allowed. For this reason it is necessary to provide repetitive output sequences from the imager. By experiment, it was determined that one line scan time should be 15.2 milliseconds. This requires a scanner clock frequency of 115.8 kHz for the 1763 pulses (35 are extra for purging and setup) of the imager.

We have now given a reason for the tape deck and the imager to run asynchronously. There is still another portion of the system whose timing must be considered. This is the rate at which the 0.005-inch Baldwin encoder pulses occur. As mentioned previously, they may not occur at a more rapid rate than data can be acquired by the tape deck. The process of loading the tape can be divided into three parts. The first sequence is the transmission and storage of the 1728 6-bit pel words from the large drum test bed (LDTB) into

the solid-state frame store memory. Once the data are in the memory, the data for the line are fed to the tape, one 6-bit word at a time, until all 1728 words for the line are stored along with a line number. An interrecord gap is then left on the tape to ensure line identity. This total three-part sequence requires about 50 milliseconds per line. This would allow 20 lines per second to be captured. Because of the jitter in the time between 0.005-inch line feed pulses, the drum was slowed to about half the maximum rate. With the belt and pulleys now on the drum, the line pulse rate is about 9.2 lines per second.

The effects of the synchronism with respect to the irregularity of images acquired must be examined. There must be a delay in acquiring a line unless the line feed pulse and the scanner start a line capture in the middle of a line. For this reason, the equipment is logically wired to accept the first complete line which begins after a line feed pulse. Since there are about seven sweeps of the imager between 0.005-inch line feed pulses, the maximum variation in position of a line scan is one-seventh of 0.005 inch or about 0.0007 inch. This is felt to be satisfactory for these tests. In real-time operation, of course, the line feed pulses will trigger the scanning mechanism.

PEL BRIGHTNESS STATISTICS

In the context of data compressibility, the pel brightness statistics are examined for the properties that differentiate black and white typed or handwritten pages from continuous tone photographs. Once this is determined, different compression algorithms may be implemented. For example, typewritten pages may be encoded with 1 bit per pel after examining the pel brightness statistics to determine the optimum threshold.

Pel brightness statistics for several of the images analyzed are presented in figures D17 through D21. Also, the pel brightness statistics in tabular form for all the images tested are given in appendix A (to this appendix). Figure D17 shows the brightness distribution for a piece of white paper with no information on it. A majority of the intensity levels fall within a very narrow range, about level 49, and there are very few pels at the other intensity levels. Figure D18 shows the brightness statistics for a typed page. Here can be seen the two-peaked curve as predicted in figure D7. The figure shows that the typewritten information centered about level 24 occupies only about 4% of the entire image. Figure D19 is another example of a typed page showing the same general characteristics of the previous one. In contrast to the typed page, figure D20 shows the brightness statistics for a continuous tone photograph containing a large number of intensity levels throughout the entire brightness range. There is no longer the two-peaked characteristic of the typed pages. However, any algorithms developed must be clever enough so as not to be fooled by dips such as those around level 16 or 22 in this figure.

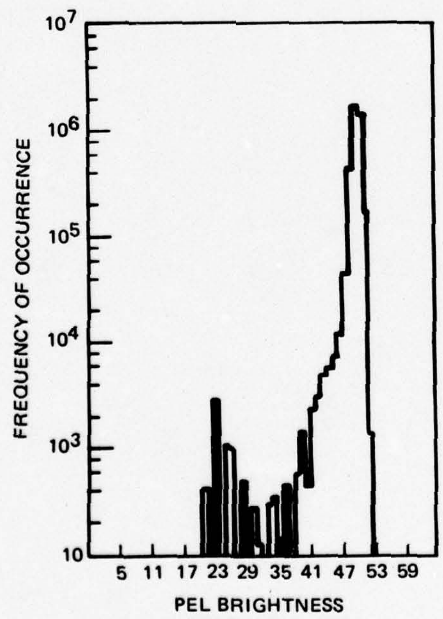

Figure D17.

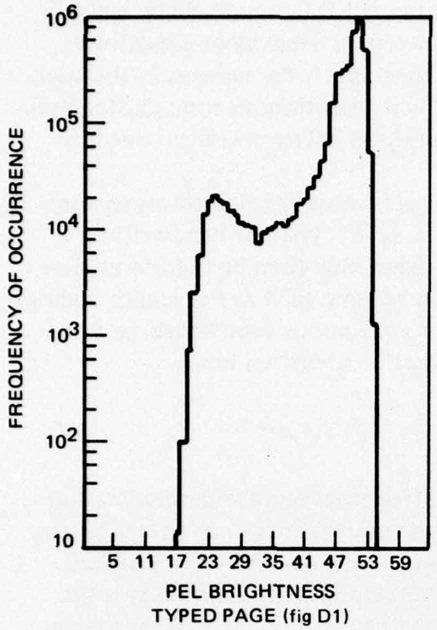

Figure D18.

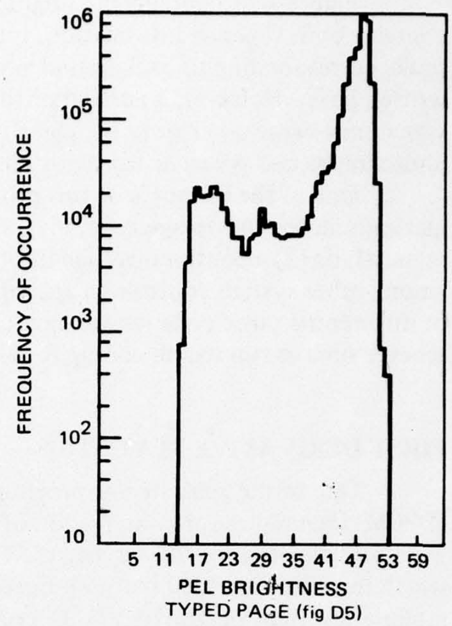

Figure D19.

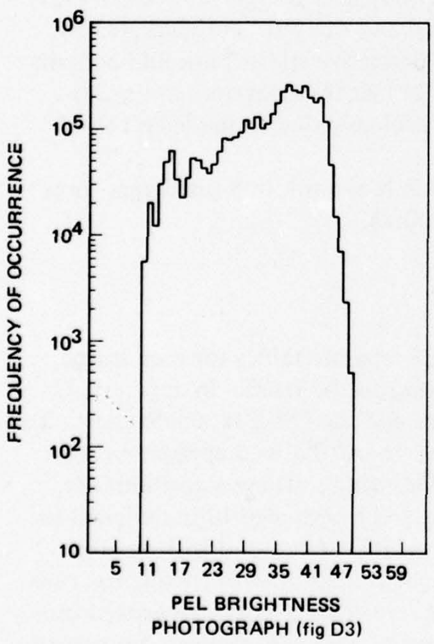

Figure D20.

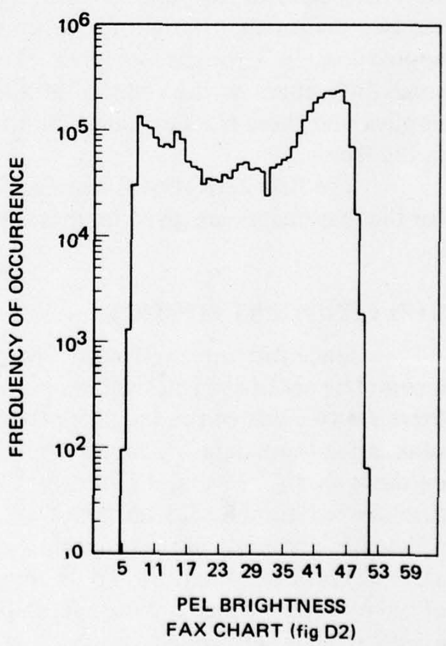

Figure D21.

Figure D21 contains the brightness statistics for the IEEE facsimile chart, which contains both types of information, typed and continuous tone. Here can be seen two peaks corresponding to background and printed information much the same as in the typewritten page. However, a portion of this chart does contain a continuous tone photograph, which may cause an error in the algorithm which differentiates between continuous tone photographs and typed or handwritten information.

One of the purposes of this program is to investigate computer algorithms to automatically determine image type; that is, whether an image is (1) typed or handwritten material, or (2) a continuous tone photograph. This decision may then be used to initiate among other system controls an appropriate compression scheme such as run length coding or differential pulse code modulation (DPCM) for a 6-bit continuous tone image, or a scheme such as run length coding for a 1-bit typewritten or handwritten image.

FIRST DERIVATIVE STATISTICS

One of the goals of this program is to examine differential pulse code modulation (DPCM) techniques for compression of these data. To do this, the first derivative statistics were accumulated for several images. Examination of these statistics showed a problem which must be corrected before proceeding with the DPCM studies. This problem is the modulation transfer function (MTF) of the large drum test bed system. A major problem is believed to be the MTF of the lens used for imaging.

Two examples of the first derivative statistics are shown in figures D22 and D23. These figures both show a predominance of changes of either 0 or 1 level, indicating little or no change in the brightness of the image. Where the data do change, the magnitude of change averages from 6 to 12 levels, as shown by the flat portions of the two curves. Referring back to the pel brightness statistics for these two images in figures D18 and D21, the two predominant brightness levels for the background and the print are separated by approximately 32 brightness levels. Therefore, the first derivative statistics should contain some differences on the order of 30 brightness levels. The fact that this does not occur implies that there is a slew rate limitation in the system probably due to the MTF roll-off in the lens.

The first derivative statistics in tabular form and in low-resolution histogram form for the test images are given in appendix B (to this appendix).

RUN LENGTH STATISTICS

Since the run length statistics are comprised of 24 separate tables for each image, a complete set of statistics will be sent under separate cover to the USPS. In appendix C there are two sets of run length statistics for a typed page and the IEEE facsimile chart. To summarize these data, a computer program was generated to calculate compression ratios on these data for several different run length encoding algorithms. These algorithms are summarized in tables D3 through D6. The first is a 6-3 fixed length algorithm designed to efficiently compress images containing a predominantly white background with smaller areas of black information. To do this, a 6-bit fixed length code is used to encode the runs of ones (white), which are in general longer than runs of zeros (black). The algorithm uses a 3-bit fixed length code to encode the shorter runs of zeros. Table D4 shows a 4-bit fixed length code which encodes both runs of ones and zeros with the same code. Table D5 shows

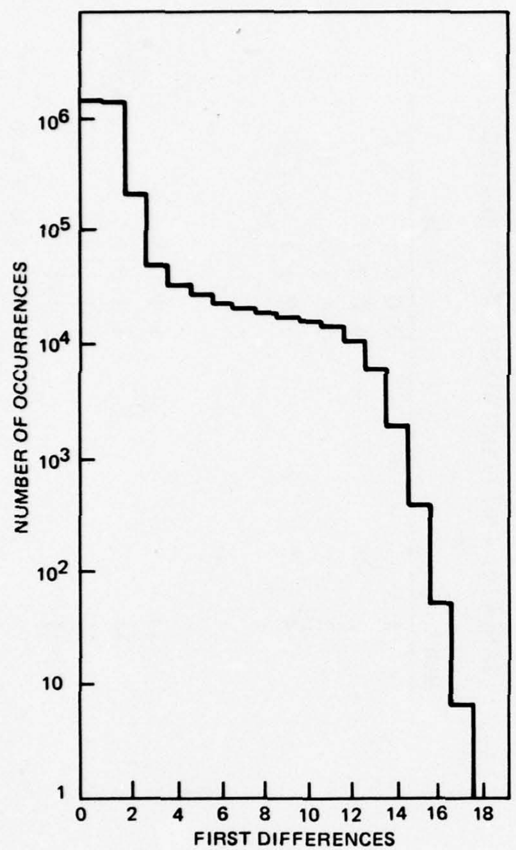

Figure D22.

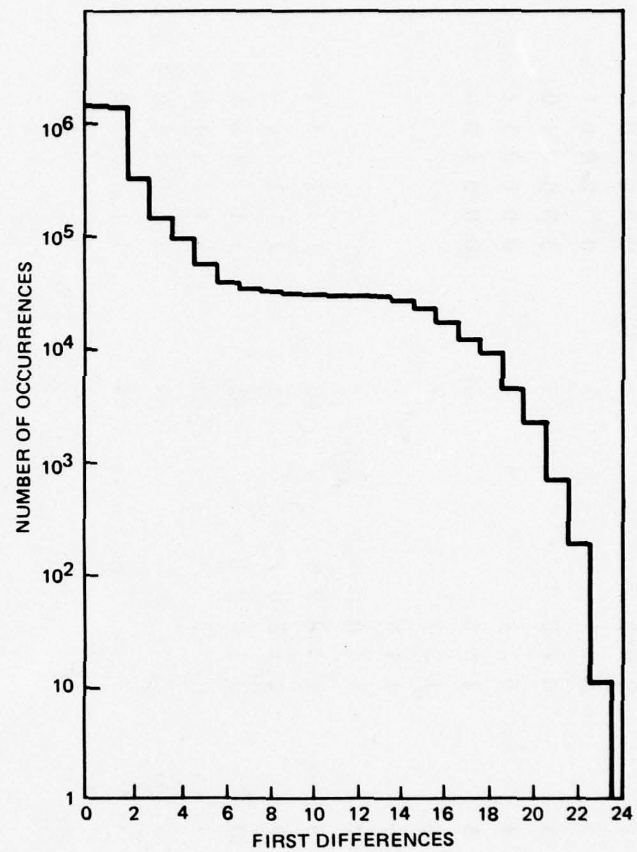

Figure D23.

TABLE D3. A 6-3 FIXED WORD LENGTH RLC CODE.

Black Runs		White Runs	
Run Length	Code	Run Length	Code
1	0 0 0	1	0 0 0 0 0 0
2	0 0 1	2	0 0 0 0 0 1
3	0 1 0	3	0 0 0 0 1 0
4	0 1 1	4	0 0 0 0 1 1
5	1 0 0	5	0 0 0 1 0 0
6	1 0 1	•	•
>6	1 1 0	•	•
7	1 1 0 0 0 0	•	•
8	1 1 0 0 0 1	60	1 1 1 0 1 1
9	1 1 0 0 1 0	61	1 1 1 1 0 0
10	1 1 0 0 1 1	62	1 1 1 1 0 1
•	•	>62	1 1 1 1 1 0
•	•	63	1 1 1 1 1 0 0 0 0 0 0 0
•	•	64	1 1 1 1 1 0 0 0 0 0 1 0
		65	1 1 1 1 1 0 0 0 0 0 1 1
		•	•
		•	•
		•	•

1 1 1 1 1 1 1 1 – SYNC

TABLE D4. 4-BIT FIXED WORD LENGTH RLC CODE.

Run Length	Code
1	0 0 0 0
2	0 0 0 1
3	0 0 1 0
4	0 0 1 1
•	•
•	•
•	•
13	1 1 0 0
14	1 1 0 1
15	1 1 1 0
>15	1 1 1 1
16	1 1 1 1 0 0 0 0
17	1 1 1 1 0 0 0 1
18	1 1 1 1 0 0 1 0
•	•
•	•
•	•

TABLE D5. VARIABLE WORD LENGTH RLC CODE WITH 3-BIT MINIMUM LENGTH CODE.

Run Length (elements)	Address	Remainder	Code Word Length (bits)
1	0	00	3
2	0	01	3
3	0	10	3
4	0	11	3
5	10	00	4
6	10	01	4
7	10	10	4
8	10	11	4
9	110	000	6
10	110	001	6
.	.	.	.
.	.	.	.
16	110	111	6
17	1110	0000	8
18	1110	0001	8
.	.	.	.
.	.	.	.
32	1110	1111	8
33	11110	00000	10
.	.	.	.
.	.	.	.
64	11110	11111	10
65	111110	000000	12
.	.	.	.
.	.	.	.
128	111110	111111	12
129	1111110	0000000	14
.	.	.	.
.	.	.	.
256	1111110	1111111	14
257	11111110	00000000	16
.	.	.	.
.	.	.	.
512	11111110	11111111	16
Margin Code	11111110		

a variable length coding scheme that begins with a 3-bit code for the shortest runs, and table D6 shows another variable length code beginning with a 2-bit sequence. The variable length codes in general give higher compression ratios at the expense of more costly hardware.

The compression ratios presented in this section should not be considered as absolute values to be obtained when implementing the specific algorithms specified here. There are two reasons for this. First, the computation of the compression ratio does not include any overhead line sync codes or header codes. A minimum length line sync code could be defined for the variable length run length code (RLC) algorithms; however, no such minimum code may be defined for the fixed length RLC algorithms. Therefore, an estimate cannot be made of the total number of overhead bits used to transmit an image. A true compression ratio must take into account all the overhead bits required for transmission. Thus, these numbers should be considered only for their relative values.

Second, since the digital image analyzer has a capability to store only 64 running totals, runs of lengths greater than 64 must be broken up into several groups. This offers no problem for the fixed length code presented here, but it does limit the effective compression ratio for variable length RLC codes. Table D6 shows a variable word length RLC dictionary for that code starting with a 2-bit word length. Depending on the particular application, an RLC encoder may be designed to encode runs up to a certain length less than 4094 shown in the table. If the encoder was designed to encode runs of not greater than 64, the results presented in this report would be an accurate indication of the compression obtained. However, the images analyzed here contain 1700 pels per line. Therefore, a run length can be as long as 1700 pels. In the most significant bit place, for example, approximately half the lines are all ones, given an image of a typed page. Using the variable word length RLC code from table D6, a run of 1700 pels can be encoded with a 20-bit code. The digital image analyzer breaks this run into 26 runs of length 64 and one run of length 36. Using the same code table these runs are encoded using a total of 322 bits, instead of 20. Therefore, the figures presented in this report should be used only to compare the relative efficiencies of the various run length compression codes.

A comparison of the compression ratios calculated for all the run length algorithms is shown in table D7 for the images tested. The compression ratios were calculated for both binary and Gray code image data. These compression ratios are computed on all 6-bit planes taken 1 bit plane at a time for each image. It is seen here that in general the compression ratios are very low and for the fixed length codes, in some cases, there is even an expansion of data rather than a compression. The main reason for this is the large number of very short runs in the lower-order bit planes. These figures also demonstrate approximately a 30% improvement in compression ratio when using Gray code instead of binary. Still another observation is that for the typed page IT3 the illumination correction procedure does improve the compressibility of the image.

For each of the four RLC algorithms examined, a comparison of the compression ratios for all the images is shown in tables D8 through D11. Since there are many very short runs in the low-order bit planes, compression ratios were computed for the images assuming a 5-bit precision and also for a 1-bit image. As can be seen in the table, there is only a slight improvement in the compressibility with 5-bit planes instead of 6. However with only the most significant bit plane there is a rather large improvement in the compression ratios shown.

TABLE D6. VARIABLE WORD LENGTH RLC CODE WITH 2-BIT MINIMUM LENGTH CODE.

Run Length (elements)	Code Word		Code Word Length
	Address	Remainder	
1	0	0	2
2	0	1	2
3	10	00	4
4	10	01	4
5	10	10	4
6	10	11	4
7	110	000	6
.	.	.	.
.	.	.	.
14	110	111	6
15	1110	0000	8
.	.	.	.
.	.	.	.
30	1110	1111	8
31	11110	00000	10
.	.	.	.
.	.	.	.
62	11110	11111	10
63	111110	000000	12
.	.	.	.
.	.	.	.
126	111110	111111	12
127	1111110	0000000	14
.	.	.	.
.	.	.	.
254	1111110	1111111	14
255	11111110	00000000	16
.	.	.	.
.	.	.	.
510	11111110	11111111	16
511	111111110	000000000	18
.	.	.	.
.	.	.	.
1022	111111110	111111111	18
1023	1111111110	0000000000	20
.	.	.	.
.	.	.	.
2046	1111111110	1111111111	20
2047	11111111110	00000000000	22
.	.	.	.
.	.	.	.
4094	11111111110	11111111111	22
MC	11111111111	111111111OP	22

TABLE D7. COMPRESSION RATIO SUMMARY.

RUN LENGTH ALGORITHM

Image Tape Number	6-3 Fixed binary	6-3 Fixed Gray	4-bit Fixed binary	4-bit Fixed Gray	3-bit Variable binary	3-bit Variable Gray	2-bit Variable binary	2-bit Variable Gray
IT2	1.00	1.37	1.85	1.53	1.56	2.02	1.70	2.10
*IT3	0.66	0.85	0.85	1.02	1.10	1.36	1.30	1.58
IT3	0.85	1.23	1.05	1.48	1.36	1.92	1.51	2.05
IT4	0.93	1.31	1.12	1.47	1.46	1.96	1.60	2.08
IT5	0.80	1.25	1.00	1.42	1.28	1.89	1.44	2.02
IT6	0.89	1.27	1.08	1.44	1.40	1.89	1.54	2.00
IT7	0.73	1.12	0.91	1.27	1.20	1.73	1.45	1.98
IT8	1.15	1.56	1.28	1.65	1.76	2.31	1.93	2.41
IT9	0.76	1.03	0.96	1.23	1.24	1.60	1.41	1.76
IT10	0.94	1.38	1.02	1.51	1.47	2.05	1.64	2.19
IT11	0.71	1.00	0.90	1.18	1.16	1.56	1.35	1.76
IT12	0.88	1.24	1.07	1.41	1.37	1.83	1.53	1.95
IT13	0.84	1.23	1.02	1.37	1.33	1.82	1.52	1.98

*Not illumination corrected

TABLE D8. 6-3 FIXED LENGTH RLC ALGORITHM COMPRESSION RATIOS.

Binary Code		6-bit Planes	5-bit Planes	MSB Plane
IT2	Typed page thresholded	1.00	1.27	3.47
IT3	Typed page white	0.85	1.02	3.53
IT4	Typed page green	0.93	1.15	3.51
IT5	Typed page red	0.80	0.94	3.50
IT6	Typed page blue	0.89	1.08	3.51
IT7	Drum photo	0.73	0.84	5.35
IT8	White paper	1.15	1.61	5.25
IT9	IEEE fax chart	0.76	0.87	2.49
IT10	USPS Announcement 771	0.94	1.17	3.80
IT11	USPS facility photo	0.71	0.79	2.38
IT12	Versatec sample print	0.88	1.06	3.04
IT13	Drum photo thresholded	0.84	1.02	4.27
Gray Code				
IT2	Typed page thresholded	1.37	1.68	3.47
IT3	Typed page white	1.28	1.60	3.53
IT4	Typed page green	1.31	1.60	3.51
IT5	Typed page red	1.25	1.51	3.50
IT6	Typed page blue	1.27	1.55	3.51
IT7	Drum photo	1.12	1.43	5.35
IT8	White paper	1.56	1.75	5.25
IT9	IEEE fax chart	1.03	1.20	2.49
IT10	USPS Announcement 771	1.38	1.66	3.80
IT11	USPS facility photo	1.00	1.20	2.38
IT12	Versatec sample print	1.24	1.50	3.04
IT13	Drum photo thresholded	1.23	1.59	4.27

TABLE D9. 4-BIT FIXED LENGTH RLC ALGORITHM COMPRESSION RATIOS.

Binary Code		6-bit Planes	5-bit Planes	MSB Plane
IT2	Typed page thresholded	1.18	1.53	2.75
IT3	Typed page white	1.04	1.30	2.79
IT4	Typed page green	1.12	1.42	2.88
IT5	Typed page red	1.00	1.22	2.79
IT6	Typed page blue	1.08	1.36	2.79
IT7	Drum photo	0.91	1.09	3.20
IT8	White paper	1.28	1.77	3.17
IT9	IEEE fax chart	0.96	1.14	2.33
IT10	USPS Announcement 771	1.12	1.43	2.86
IT11	USPS facility photo	0.99	1.05	2.22
IT12	Versatec sample print	1.07	1.33	2.61
IT13	Drum photo thresholded	1.02	1.29	2.95
Gray Code				
IT2	Typed page thresholded	1.53	1.85	2.75
IT3	Typed page white	1.45	1.77	2.79
IT4	Typed page green	1.47	1.77	2.88
IT5	Typed page red	1.42	1.71	2.79
IT6	Typed page blue	1.44	1.75	2.79
IT7	Drum photo	1.27	1.60	3.20
IT8	White paper	1.65	1.86	3.17
IT9	IEEE fax chart	1.23	1.44	2.33
IT10	USPS Announcement 771	1.51	1.81	2.86
IT11	USPS facility photo	1.18	1.43	2.22
IT12	Versatec sample print	1.41	1.71	2.61
IT13	Drum photo thresholded	1.37	1.75	2.95

TABLE D10. 3-BIT VARIABLE LENGTH RLC ALGORITHM COMPRESSION RATIOS.

Binary Code		6-bit Planes	5-bit Planes	MSB Plane
IT2	Typed page thresholded	1.56	2.04	4.32
IT3	Typed page white	1.36	1.70	4.35
IT4	Typed page green	1.46	1.87	4.33
IT5	Typed page red	1.28	1.57	4.32
IT6	Typed page blue	1.40	1.78	4.33
IT7	Drum photo	1.20	1.46	6.30
IT8	White paper	1.76	2.56	6.23
IT9	IEEE fax chart	1.24	1.48	3.25
IT10	USPS Announcement 771	1.47	1.90	4.70
IT11	USPS facility photo	1.16	1.36	3.30
IT12	Versatec sample print	1.37	1.70	3.76
IT13	Drum photo thresholded	1.33	1.68	5.10
Gray Code				
IT2	Typed page thresholded	2.02	2.52	4.32
IT3	Typed page white	1.92	2.44	4.35
IT4	Typed page green	1.96	2.46	4.33
IT5	Typed page red	1.89	2.37	4.32
IT6	Typed page blue	1.89	2.36	4.33
IT7	Drum photo	1.73	2.27	6.30
IT8	White paper	2.31	2.77	6.23
IT9	IEEE fax chart	1.60	1.92	3.25
IT10	USPS Announcement 771	2.05	2.56	4.70
IT11	USPS facility photo	1.56	1.94	3.30
IT12	Versatec sample print	1.83	2.28	3.76
IT13	Drum photo thresholded	1.82	2.39	5.10

TABLE D11. 2-BIT VARIABLE LENGTH RLC ALGORITHM COMPRESSION RATIOS.

Binary Code		6-bit Planes	5-bit Planes	MSB Plane
IT2	Typed page thresholded	1.70	2.13	3.87
IT3	Typed page white	1.51	1.82	3.77
IT4	Typed page green	1.60	1.96	3.74
IT5	Typed page red	1.44	1.71	3.72
IT6	Typed page blue	1.54	1.87	3.74
IT7	Drum photo	1.45	1.72	5.28
IT8	White paper	1.93	2.64	5.22
IT9	IEEE fax chart	1.41	1.64	2.98
IT10	USPS Announcement 771	1.64	2.04	4.11
IT11	USPS facility photo	1.35	1.56	3.29
IT12	Versatec sample print	1.52	1.84	3.46
IT13	Drum photo thresholded	1.52	1.84	4.51
Gray Code				
IT2	Typed page thresholded	2.10	2.53	3.87
IT3	Typed page white	2.05	2.49	3.77
IT4	Typed page green	2.08	2.51	3.74
IT5	Typed page red	2.02	2.44	3.72
IT6	Typed page blue	2.00	2.41	3.74
IT7	Drum photo	1.98	2.50	5.28
IT8	White paper	2.41	2.81	5.22
IT9	IEEE fax chart	1.76	2.03	2.98
IT10	USPS Announcement 771	2.19	2.63	4.11
IT11	USPS facility photo	1.76	2.13	3.29
IT12	Versatec sample print	1.95	2.36	3.46
IT13	Drum photo thresholded	1.98	2.49	4.51

RESULTS AND CONCLUSIONS

1. Three types of statistics were obtained from 13 image data files – pel brightness statistics, first derivative statistics, and run length statistics. These statistics are presented in tabular form for selected images in appendices A, B, and C.

2. The pel brightness statistics show overall similarities for two distinct image types – typewritten pages and continuous photographs. The possibility does exist that an algorithm can be generated to differentiate between these image types.

3. The first derivative statistics brought to the surface a problem associated with the large drum test bed. This problem resulted in a lack of pel-to-pel differences of an expected magnitude, that magnitude being the difference between the average white level and the average black level in an image. It is believed that the imaging lens has too low a modulation transfer function (MTF) for imaging at 200 by 200 pels per inch.

4. The run length statistics show a very large number of very short runs in the lower bit planes, resulting in relatively low compression ratios. A large part of this is caused by an unbalanced condition in the two analog transport registers in the CCD-121 imager. A newly designed imager, CCD-121H, is supposed to eliminate this problem. However, the compression ratios presented in this report do indicate several things:

a. Variable length RLC algorithms exhibit higher compression ratios than fixed length codes.

b. For the fixed length codes the 4-bit algorithm unexpectedly showed slightly higher compression ratios than the 6-3 fixed algorithm. This is believed to be due to the large number of very short runs. For the most significant bit plane only, representing a 1-bit image, the 6-3 fixed length algorithm is about 20% better.

c. For the variable length codes the 2-bit code – ie, the code which begins with a 2-bit minimum length code word – shows slightly higher compression ratios for all 6-bit planes. However, for only the most significant bit plane the opposite is true. Again, this is due to the large number of short runs in the lower bit planes.

d. Converting the image data from binary to Gray code produces about a 30% increase in compression ratios from all the algorithms.

PLANNED FUTURE NELC ACTIVITIES

1. The newly designed CCD-121HC (1728 element) and the CCD-131DC (1024 element) imaging devices will be integrated into the large drum test bed for future image acquisition and analysis.

2. If one can be obtained, a new imaging lens with a higher modulation transfer function (MTF) will be installed on the large drum test bed.

3. To obtain a more accurate representation of compressibility using the variable length RLC algorithms, a software program or hardware modification should be generated so that runs longer than 64 bits (up to 1728 bits) can be detected and tallied.

4. The applicability of differential pulse code modulation (DPCM) compression techniques to USPS images will be studied.

5. Novel compression techniques such as block void coding and special run length routines will be investigated.

APPENDIX A (TO TR2020 APPENDIX D):

TABULAR BINARY PEL BRIGHTNESS STATISTICS FOR IMAGE TAPES IT2 THROUGH IT13

0	0	16	0	32	10295	48	12916
1	0	17	0	33	10679	49	16216
2	0	18	0	34	3724	50	21036
3	0	19	3	35	3881	51	29585
4	0	20	41	36	7991	52	39429
5	0	21	312	37	7377	53	56078
6	0	22	1437	38	7228	54	92159
7	0	23	3737	39	7126	55	167570
8	0	24	5839	40	7066	56	240384
9	0	25	10673	41	5279	57	273146
10	0	26	15534	42	7380	58	269676
11	0	27	17337	43	7935	59	372240
12	0	28	16447	44	7738	60	366804
13	0	29	15644	45	7796	61	324309
14	0	30	19289	46	3976	62	438892
15	0	31	16443	47	11085	63	162268

TYPED PAGE THRESHOLDED - NO FILTER - *IT2/2* - 10 NOV 1976 - MODE 0

0	0	16	311	32	19875	48	131990
1	0	17	1304	33	53427	49	51515
2	0	18	4015	34	71503	50	5557
3	0	19	5946	35	70466	51	16
4	0	20	17429	36	102843	52	0
5	0	21	24181	37	138744	53	0
6	0	22	13954	38	141319	54	0
7	0	23	16234	39	149060	55	0
8	0	24	19610	40	131733	56	0
9	0	25	16006	41	311435	57	0
10	0	26	13010	42	432977	58	0
11	0	27	9460	43	460309	59	0
12	1	28	12597	44	355203	60	0
13	1	29	12485	45	347042	61	0
14	11	30	13561	46	156772	62	0
15	19	31	12732	47	135524	63	0

TYPED PAGE UNCORRECTED - WHITE - *IT3/1* - 03 NOVEMBER 1976 - MODE 0

BEST AVAILABLE COPY

1	0	17	0	33	7253	49	318374
2	0	18	13	34	9489	50	334113
3	0	19	22	35	10077	51	712975
4	0	20	730	36	10401	52	959216
5	0	21	2469	37	11350	53	464338
6	0	22	5731	38	10989	54	53024
7	0	23	13701	39	12398	55	1247
8	0	24	19058	40	13185	56	5
9	0	25	22002	41	17933	57	0
10	0	26	18265	42	19057	58	0
11	0	27	17767	43	24451	59	0
12	0	28	14940	44	32106	60	0
13	0	29	13911	45	43712	61	0
14	0	30	11394	46	65000	62	0
15	0	31	10914	47	152200	63	0
16	0	32	10564	48	294500	64	0

TYPED PAGE - WHITE - *IT3/2* - 02 NOVEMBER 1976 - MODE 0

0	0	16	75	32	6751	48	382204
1	0	17	563	33	3681	49	502994
2	0	18	2517	34	3600	50	799213
3	0	19	6479	35	3254	51	586353
4	0	20	10427	36	3512	52	210540
5	0	21	19026	37	10736	53	26136
6	0	22	21149	38	13389	54	621
7	0	23	19662	39	14955	55	0
8	0	24	15705	40	17920	56	0
9	0	25	15624	41	21490	57	0
10	0	26	12937	42	30335	58	0
11	0	27	11360	43	45168	59	0
12	0	28	9241	44	75245	60	0
13	0	29	9693	45	132234	61	0
14	0	30	9637	46	233776	62	0
15	0	31	9077	47	319639	63	0

TYPED PAGE - GREEN FILTER - *IT4/2* - 05 NOVEMBER 1976 - MODE 0

1	0	17	1363	33	6891	49	654527
2	0	18	3642	34	7337	50	592901
3	0	19	13107	35	10522	51	375213
4	0	20	17791	36	11256	52	37295
5	0	21	18831	37	12201	53	3544
6	0	22	20948	38	11895	54	1
7	0	23	18095	39	15288	55	0
8	0	24	14951	40	12927	56	0
9	0	25	10930	41	13738	57	0
10	0	26	10675	42	14647	58	0
11	0	27	10496	43	71288	59	0
12	0	28	9175	44	147207	60	0
13	0	29	3760	45	161145	61	0
14	10	30	3695	46	222703	62	0
15	129	31	3204	47	341601	63	0
16	345	32	3108	48	511682	64	0

TYPED PAGE - RED FILTER - SITE 2* - 12 NOVEMBER 1976 - MODE 0

0	0	16	2986	32	5556	48	138847
1	0	17	3345	33	7738	49	327747
2	0	18	13611	34	7340	50	727153
3	0	19	17564	35	9911	51	282264
4	0	20	15243	36	9257	52	318954
5	0	21	16827	37	9458	53	568253
6	0	22	17313	38	10298	54	199424
7	0	23	13564	39	12132	55	25576
8	0	24	11790	40	13833	56	1273
9	0	25	9982	41	15561	57	1
10	0	26	9514	42	17387	58	1
11	0	27	8296	43	21994	59	0
12	1	28	7793	44	27332	60	0
13	50	29	7249	45	37429	61	0
14	427	30	7444	46	55515	62	0
15	1317	31	7344	47	107591	63	0

TYPED PAGE - BLUE FILTER - SITE 2* - 09 NOVEMBER 1976 - MODE 0

1	0	17	103458	33	5	49	0
2	0	18	96682	34	1	50	0
3	0	19	112320	35	1	51	0
4	0	20	101423	36	0	52	0
5	457	21	97260	37	0	53	0
6	2732	22	103115	38	0	54	0
7	197486	23	93276	39	0	55	0
8	552057	24	49147	40	0	56	0
9	482763	25	33865	41	0	57	0
10	484291	26	24021	42	0	58	0
11	315551	27	18291	43	0	59	0
12	322825	28	14587	44	0	60	0
13	165553	29	2386	45	0	61	0
14	188108	30	2864	46	0	62	0
15	138302	31	710	47	0	63	0
16	129430	32	29	48	0	64	0

PHOTOGRAPH OF LARGE DRUM - WHITE - KIT7/2% - 03 NOV 1976 - MODE 0

1	0	17	0	33	3	49	140678
2	0	18	1	34	311	50	1640097
3	0	19	0	35	361	51	1401718
4	0	20	1	36	17	52	157911
5	0	21	1	37	457	53	1794
6	0	22	431	38	57	54	0
7	0	23	7	39	581	55	0
8	0	24	1917	40	1433	56	0
9	0	25	15	41	438	57	0
10	0	26	1084	42	1380	58	0
11	0	27	1003	43	1035	59	0
12	0	28	1	44	4880	60	0
13	0	29	520	45	5744	61	0
14	0	30	5	46	7264	62	0
15	0	31	197	47	12159	63	0
16	0	32	127	48	14640	64	0

WHITE PAPER - NO FILTER - KIT8/2% - 05 NOVEMBER 1976 - MODE 0

0	0	16	34531	32	24365	48	51483
1	0	17	30498	33	45785	49	16229
2	0	18	46554	34	47963	50	1854
3	0	19	43390	35	52438	51	56
4	3	20	31544	36	53067	52	0
5	36	21	35660	37	70246	53	0
6	1317	22	34590	38	35593	54	0
7	31400	23	32765	39	127765	55	0
8	136356	24	37878	40	152501	56	0
9	110482	25	35276	41	183085	57	0
10	107620	26	42412	42	201039	58	0
11	85297	27	40856	43	225829	59	0
12	69991	28	30446	44	225632	60	0
13	74749	29	43376	45	234169	61	0
14	80670	30	43460	46	239108	62	0
15	87413	31	41575	47	185510	63	0

IEEE FACS CHART - NO FILTER - BIT9/2* - 03 NOVEMBER 1976 - MODE 0

0	0	16	1564	32	10851	48	164053
1	0	17	17242	33	3049	49	335528
2	0	18	23236	34	7616	50	350730
3	0	19	18561	35	3068	51	277467
4	0	20	19163	36	3195	52	25424
5	0	21	23628	37	3101	53	701
6	0	22	20334	38	9459	54	396
7	0	23	14080	39	12882	55	0
8	0	24	10438	40	19142	56	0
9	0	25	7373	41	15388	57	0
10	0	26	7513	42	32499	58	0
11	0	27	5733	43	37020	59	0
12	0	28	7590	44	60490	60	0
13	0	29	6043	45	115515	61	0
14	10	30	14916	46	118211	62	0
15	735	31	9911	47	388514	63	0

TYPED PAGE (USPS #771) - WHITE - BIT10/2* - 05 NOV 1976 - MODE 0

0	0	16	33978	32	39950	48	2353
1	0	17	22887	33	110886	49	504
2	0	18	33895	34	136618	50	3
3	0	19	54342	35	176898	51	0
4	0	20	50393	36	228619	52	0
5	0	21	43195	37	262959	53	0
6	0	22	37912	38	231142	54	0
7	0	23	47653	39	229726	55	0
8	0	24	61828	40	261063	56	0
9	5	25	30549	41	202059	57	0
10	5602	26	79154	42	179789	58	0
11	20983	27	33251	43	191168	59	0
12	12132	28	21862	44	119990	60	0
13	30220	29	102728	45	46422	61	0
14	49078	30	100188	46	15230	62	0
15	63973	31	131654	47	7168	63	0

USPS FACILITY - NO FILTER - KIT11/2* - 03 NOVEMBER 1976 MODE 0

0	0	16	0	32	14483	48	167237
1	0	17	2	33	15867	49	29956
2	0	18	204	34	18230	50	214
3	0	19	1764	35	19115	51	19
4	0	20	5804	36	18719	52	2
5	0	21	14297	37	17611	53	5
6	0	22	24305	38	19910	54	3
7	0	23	27676	39	24100	55	5
8	0	24	26871	40	29198	56	0
9	0	25	28490	41	32704	57	0
10	0	26	29962	42	55243	58	0
11	0	27	27884	43	159872	59	0
12	0	28	25548	44	514165	60	0
13	0	29	21652	45	393388	61	0
14	0	30	21420	46	379043	62	0
15	0	31	19024	47	557100	63	0

VERSATEC PRINT - NO FILTER - KIT12/2* - 04 NOVEMBER 1976 - MODE 0

0	0	16	145011	32	33952	48	12978
1	0	17	140313	33	45640	49	12430
2	0	18	109487	34	43832	50	10651
3	0	19	36375	35	44484	51	10779
4	0	20	76930	36	45421	52	10062
5	0	21	77430	37	45523	53	3929
6	0	22	59100	38	50798	54	3455
7	25	23	56927	39	50478	55	2922
8	78171	24	56443	40	50399	56	3678
9	194418	25	50395	41	48522	57	2949
10	429013	26	59767	42	35868	58	2060
11	296645	27	54256	43	23416	59	1932
12	275912	28	52197	44	16630	60	1805
13	227123	29	51178	45	14179	61	1647
14	193892	30	48611	46	13172	62	1556
15	170079	31	49203	47	14161	63	42891

PHOTOGRAPH - THRESHOLDED - NO FILTER - KIT13/2* - 08 NOV 1976 - MODE 0

APPENDIX B (TO TR2020 APPENDIX D):

TABULAR BINARY FIRST
DERIVATIVE STATISTICS
FOR
IMAGE TAPES IT2 THROUGH IT13

0	1762912	16	19707	32	147	48	0
1	1511231	17	3246	33	12	49	0
2	178090	18	7056	34	0	50	0
3	47465	19	1552	35	10	51	0
4	71270	20	391	36	77	52	0
5	24552	21	159	37	0	53	0
6	20253	22	45	38	11	54	0
7	18163	23	1	39	0	55	0
8	16572	24	0	40	5	56	0
9	15052	25	0	41	0	57	0
10	13814	26	0	42	0	58	0
11	12885	27	1	43	0	59	0
12	12581	28	0	44	0	60	0
13	12655	29	34	45	0	61	1
14	12215	30	1156	46	0	62	0
15	12247	31	0	47	0	63	7375

TYPED PAGE THRESHOLDED - NO FILTER - KIT3 1* - 10 NOV 1976 - MODE -

0	312116	16	0	32	734	48	0
1	1446078	17	1	33	19	49	0
2	716481	18	1	34	0	50	0
3	104166	19	0	35	0	51	0
4	174151	20	1	36	0	52	0
5	51904	21	1	37	0	53	0
6	28782	22	1	38	0	54	0
7	14364	23	2	39	0	55	0
8	11830	24	1	40	0	56	0
9	19215	25	5	41	0	57	0
10	16276	26	0	42	0	58	0
11	12376	27	0	43	0	59	0
12	7232	28	2	44	0	60	0
13	2221	29	3	45	0	61	0
14	525	30	194	46	0	62	0
15	37	31	346	47	0	63	0

TYPED PAGE UNCORRECTED - WHITE - KIT3/1* - 03 NOVEMBER 1976 - MODE -

0	1611524	16	68	32	0	48	346
1	1608985	17	7	33	1	49	0
2	344159	18	0	34	2	50	794
3	58297	19	2	35	0	51	0
4	38417	20	2	36	2	52	29
5	30855	21	0	37	2	53	0
6	25718	22	1	38	0	54	0
7	23210	23	3	39	5	55	0
8	20951	24	0	40	0	56	0
9	19392	25	1	41	0	57	0
10	18255	26	0	42	0	58	0
11	16266	27	1	43	0	59	0
12	12256	28	1	44	2	60	0
13	6876	29	0	45	3	61	0
14	3132	30	0	46	0	62	0
15	432	31	1	47	194	63	0

TYPED PAGE - WHITE - *IT3/2* - 02 NOVEMBER 1976 - MODE -

0	1679504	16	2637	32	38	48	0
1	1563304	17	329	33	0	49	326
2	323389	18	333	34	282	50	0
3	56599	19	43	35	131	51	0
4	36435	20	3	36	0	52	1
5	28134	21	0	37	143	53	0
6	23708	22	0	38	0	54	0
7	20493	23	0	39	142	55	0
8	19000	24	3	40	190	56	0
9	17036	25	1	41	0	57	0
10	15958	26	0	42	114	58	0
11	14208	27	255	43	0	59	0
12	12914	28	0	44	112	60	0
13	10431	29	115	45	102	61	0
14	7841	30	42	46	0	62	0
15	5001	31	0	47	150	63	0

TYPED PAGE - GREEN FILTER - *IT4/2* - 05 NOVEMBER 1976 - MODE -

0	1559496	16	2383	32	0	48	0
1	1542132	17	731	33	37	49	0
2	149956	18	108	34	39	50	0
3	53337	19	11	35	0	51	0
4	42957	20	2	36	54	52	0
5	32070	21	0	37	0	53	0
6	23986	22	1	38	57	54	0
7	19013	23	37	39	186	55	0
8	17772	24	0	40	0	56	0
9	16557	25	433	41	371	57	0
10	15273	26	137	42	0	58	0
11	14710	27	0	43	166	59	0
12	13946	28	73	44	191	60	0
13	12674	29	7	45	0	61	0
14	9244	30	0	46	172	62	0
15	5491	31	53	47	16	63	0

TYPED PAGE - RED FILTER - IT5/2* - 12 NOVEMBER 1976 - MODE 7

0	1600557	16	7444	32	0	48	337
1	1593553	17	5873	33	1	49	349
2	253098	18	3867	34	0	50	519
3	56412	19	3417	35	10	51	0
4	36099	20	1171	36	0	52	31
5	27102	21	431	37	30	53	0
6	22277	22	120	38	103	54	0
7	19316	23	35	39	0	55	0
8	17880	24	1	40	15	56	0
9	16434	25	2	41	38	57	0
10	14728	26	5	42	35	58	0
11	13767	27	2	43	0	59	0
12	12962	28	0	44	33	60	0
13	12481	29	0	45	262	61	0
14	10726	30	1	46	171	62	0
15	9058	31	0	47	0	63	0

TYPED PAGE - BLUE FILTER - *IT6/2* - 09 NOVEMBER 1976 - MODE 7

0	1280799	16	155	32	0	48	0
1	1639849	17	0	33	0	49	0
2	505408	18	76	34	0	50	0
3	213505	19	172	35	0	51	0
4	39760	20	1	36	0	52	0
5	7592	21	30	37	0	53	0
6	521	22	14	38	0	54	0
7	155	23	0	39	0	55	0
8	54	24	15	40	0	56	0
9	39	25	0	41	0	57	0
10	305	26	27	42	0	58	0
11	269	27	39	43	0	59	0
12	0	28	1	44	0	60	0
13	560	29	140	45	0	61	0
14	273	30	1	46	0	62	0
15	0	31	0	47	0	63	0

PHOTOGRAPH OF LARGE DRUM - WHITE - KIT7/2* - 03 NOV 1976 - MODE 7

0	1812070	16	0	32	0	48	0
1	1731474	17	0	33	0	49	0
2	178413	18	0	34	0	50	0
3	7263	19	0	35	0	51	0
4	1295	20	0	36	0	52	0
5	2119	21	154	37	0	53	0
6	739	22	0	38	0	54	0
7	435	23	1170	39	0	55	0
8	515	24	0	40	0	56	0
9	737	25	458	41	0	57	0
10	788	26	137	42	0	58	0
11	336	27	0	43	0	59	0
12	331	28	70	44	0	60	0
13	102	29	0	45	0	61	0
14	12	30	11	46	0	62	0
15	1	31	0	47	0	63	0

WHITE PAPER - NO FILTER - KIT8/2* - 05 NOVMBER 1976 - MODE 7

0	1423105	16	16867	32	2	48	0
1	1367457	17	12101	33	0	49	159
2	311006	18	3716	34	1	50	0
3	143379	19	1456	35	1	51	0
4	91376	20	2144	36	0	52	0
5	54639	21	590	37	0	53	0
6	38723	22	189	38	0	54	0
7	34281	23	11	39	0	55	0
8	31623	24	2195 10	40	2	56	0
9	31118	25	5	41	0	57	0
10	30007	26	0	42	104	58	0
11	29709	27	13	43	0	59	0
12	29472	28	0	44	395	60	0
13	28737	29	1	45	0	61	0
14	25526	30	0	46	410	62	0
15	22473	31	0	47	292	63	0

IEEE FACS CHART - NO FILTER - *IT9/2* - 03 NOVEMBER 1976 - MODE 7

0	1703873	16	1408	32	77	48	0
1	1613428	17	183	33	10	49	0
2	237382	18	123	34	0	50	0
3	50069	19	13	35	31	51	0
4	25964	20	0	36	18	52	0
5	18023	21	0	37	0	53	0
6	14516	22	0	38	0	54	0
7	12792	23	0	39	0	55	0
8	10520	24	0	40	0	56	0
9	9925	25	0	41	0	57	0
10	8462	26	0	42	0	58	0
11	7738	27	1	43	0	59	0
12	7465	28	0	44	0	60	0
13	6920	29	128	45	0	61	0
14	5465	30	1897	46	0	62	0
15	5341	31	0	47	0	63	0

TYPED PAGE (USPS #771) - WHITE - *IT10/2* - 05 NOV 1976 - MODE -

0	1206547	16	0	32	0	48	0
1	1362054	17	0	33	0	49	0
2	555329	18	0	34	0	50	0
3	375613	19	0	35	0	51	0
4	182107	20	0	36	0	52	0
5	43577	21	0	37	0	53	0
6	7407	22	0	38	0	54	0
7	2692	23	0	39	0	55	0
8	1245	24	0	40	0	56	0
9	525	25	2036	41	0	57	0
10	522	26	0	42	0	58	0
11	75	27	36	43	0	59	0
12	7	28	51	44	0	60	0
13	0	29	0	45	0	61	0
14	0	30	0	46	0	62	0
15	0	31	17	47	0	63	0

USPS FACILITY - NO FILTER - *IT11/2* - 03 NOVEMBER 1976 MODE 7

0	1565844	16	514	32	30	48	0
1	1540992	17	44	33	0	49	0
2	180327	18	1	34	1	50	0
3	76999	19	5	35	0	51	0
4	48367	20	1	36	0	52	0
5	38814	21	0	37	0	53	0
6	33634	22	0	38	0	54	0
7	30392	23	0	39	0	55	0
8	27575	24	0	40	0	56	0
9	24781	25	0	41	0	57	0
10	20325	26	198	42	0	58	0
11	17314	27	1593	43	0	59	0
12	14176	28	0	44	0	60	0
13	10028	29	120	45	0	61	0
14	5509	30	0	46	0	62	0
15	2155	31	50	47	0	63	0

VERSATEC PRINT - NO FILTER - *IT12/2* - 04 NOVEMBER 1976 - MODE 7

0	1379321	16	0	32	55	48	0
1	1717715	17	193	33	30	49	22
2	800232	18	135	34	0	50	38
3	39295	19	0	35	67	51	0
4	22554	20	305	36	52	52	27
5	3624	21	135	37	0	53	17
6	4175	22	0	38	70	54	0
7	2423	23	59	39	0	55	36
8	1383	24	30	40	10	56	19
9	375	25	0	41	12	57	0
10	511	26	34	42	0	58	3
11	294	27	52	43	16	59	0
12	125	28	0	44	36	60	0
13	60	29	12	45	0	61	1
14	21	30	50	46	22	62	0
15	36	31	0	47	14	63	199

PHOTOGRAPH - THRESHOLDED - NO FILTER - RIT13/2* - 08 NOV 1976 - MODE 7

APPENDIX C (TO APPENDIX D):

TABULAR BINARY AND GRAY RUN LENGTH STATISTICS FOR IMAGE TAPES IT3/2 AND IT9/2

00	PBS	BINARY			BLACK
01	BRLS	0s	BP	1	BLACK
02	BRLS	0s	BP	2	BLACK
03	BRLS	0s	BP	3	BLACK
04	BRLS	0s	BP	4	BLACK
05	BRLS	0s	BP	5	BLACK
06	BRLS	0s	BP	6	BLACK
07	FDS	BINARY			
10	PBS	BINARY	SUBTRACT		WHITE
11	BRLS	1s	BP	1	WHITE
12	BRLS	1s	BP	2	WHITE
13	BRLS	1s	BP	3	WHITE
14	BRLS	1s	BP	4	WHITE
15	BRLS	1s	BP	5	WHITE
16	BRLS	1s	BP	6	WHITE
17	(NOT USED)				
20	PBS	GRAY CODE			BLACK
21	GRLS	0s	BP	1	BLACK
22	GRLS	0s	BP	2	BLACK
23	GRLS	0s	BP	3	BLACK
24	GRLS	0s	BP	4	BLACK
25	GRLS	0s	BP	5	BLACK
26	GRLS	0s	BP	6	BLACK
27	FDS	GRAY			
30	PBS	GRAY	SUBTRACT		WHITE
31	GRLS	1s	BP	1	WHITE
32	GRLS	1s	BP	2	WHITE
33	GRLS	1s	BP	3	WHITE
34	GRLS	1s	BP	4	WHITE
35	GRLS	1s	BP	5	WHITE
36	GRLS	1s	BP	6	WHITE
37	(NOT USED)				

PBS = PEL BRIGHTNESS STATS
BRLS = BINARY RUN LENGTH STATS
FDS = FIRST DIFFERENCE STATS
GRLS = GRAY RUN LENGTH STATS
BP = BIT PLANE NUMBER
BP 1 = LSB
BP 6 = MSB

ANALYZER MODES

1	462100	17	147	33	0	49	0
2	184714	18	107	34	0	50	0
3	109769	19	32	35	1	51	0
4	54598	20	28	36	0	52	0
5	30302	21	14	37	0	53	0
6	14531	22	14	38	0	54	0
7	10596	23	12	39	0	55	0
8	5820	24	16	40	0	56	0
9	3839	25	5	41	0	57	0
10	2282	26	3	42	0	58	0
11	1617	27	1	43	0	59	0
12	372	28	1	44	0	60	0
13	783	29	2	45	0	61	0
14	371	30	1	46	0	62	0
15	289	31	0	47	0	63	0
16	321	32	0	48	0	64	0

TYPED PAGE - WHITE - KIT3/2* - 02 NOVEMBER 1976 - MODE 1

1	333758	17	353	33	115	49	35
2	31619	18	597	34	95	50	36
3	58778	19	555	35	76	51	17
4	25287	20	396	36	76	52	30
5	19479	21	468	37	96	53	18
6	3540	22	303	38	53	54	17
7	3577	23	348	39	58	55	20
8	4616	24	309	40	47	56	15
9	5017	25	290	41	58	57	13
10	3647	26	230	42	57	58	14
11	3329	27	269	43	52	59	16
12	1744	28	172	44	41	60	3
13	1737	29	136	45	30	61	3
14	1085	30	157	46	15	62	12
15	1245	31	142	47	26	63	11
16	356	32	116	48	29	64	142

TYPED PAGE - WHITE - KIT3/2* - 02 NOVEMBER 1976 - MODE 2

1	108972	17	1679	33	483	49	199
2	62421	18	1553	34	335	50	153
3	46959	19	1369	35	408	51	252
4	21097	20	328	36	325	52	171
5	18882	21	1007	37	351	53	213
6	3792	22	706	38	273	54	167
7	10497	23	725	39	365	55	202
8	5447	24	471	40	329	56	149
9	6194	25	301	41	356	57	177
10	3307	26	366	42	277	58	175
11	4265	27	357	43	277	59	199
12	2300	28	463	44	199	60	172
13	3023	29	517	45	348	61	200
14	1943	30	463	46	237	62	114
15	2015	31	523	47	376	63	191
16	1407	32	353	48	245	64	11921

TYPED PAGE - WHITE - *IT3/2* - 02 NOVEMBER 1976 - MODE 3

1	116752	17	484	33	157	49	156
2	22337	18	347	34	147	50	36
3	17685	19	435	35	153	51	39
4	6332	20	253	36	498	52	38
5	6166	21	327	37	147	53	30
6	3087	22	189	38	181	54	136
7	3359	23	279	39	170	55	39
8	1633	24	190	40	154	56	30
9	2015	25	281	41	143	57	109
10	1082	26	182	42	153	58	35
11	1378	27	239	43	170	59	76
12	307	28	181	44	204	60	36
13	1031	29	189	45	178	61	79
14	567	30	149	46	191	62	103
15	769	31	179	47	110	63	39
16	369	32	181	48	132	64	35315

TYPED PAGE - WHITE - *IT3/2* - 02 NOVEMBER 1976 - MODE 4

1	35761	17	397	33	128	49	12
2	16531	18	762	34	117	50	3
3	16996	19	570	35	110	51	15
4	10513	20	450	36	31	52	3
5	3431	21	410	37	35	53	11
6	7045	22	293	38	72	54	17
7	6378	23	219	39	65	55	14
8	4158	24	193	40	58	56	5
9	3549	25	152	41	51	57	10
10	2929	26	184	42	31	58	10
11	2745	27	198	43	25	59	13
12	2207	28	212	44	22	60	7
13	2073	29	225	45	21	61	3
14	1511	30	188	46	12	62	1
15	1454	31	158	47	19	63	11
16	1168	32	141	48	17	64	359

TYPED PAGE - WHITE - KIT3/2* - 02 NOVEMBER 1976H MODE 5

1	1181	17	0	33	0	49	0
2	7528	18	0	34	0	50	0
3	20638	19	0	35	0	51	0
4	4719	20	0	36	0	52	0
5	1816	21	0	37	0	53	0
6	1122	22	0	38	0	54	0
7	1048	23	0	39	0	55	0
8	317	24	0	40	0	56	0
9	304	25	0	41	0	57	0
10	397	26	0	42	0	58	0
11	792	27	0	43	0	59	0
12	309	28	0	44	0	60	0
13	315	29	0	45	0	61	0
14	74	30	0	46	0	62	0
15	31	31	0	47	0	63	0
16	7	32	0	48	0	64	0

TYPED PAGE - WHITE - KIT3/2* - 02 NOVEMBER 1976 - MODE 6

1	160999	17	36	33	0	49	0
2	183167	18	50	34	0	50	0
3	105138	19	19	35	0	51	0
4	55009	20	19	36	0	52	0
5	12574	21	12	37	0	53	0
6	15980	22	17	38	0	54	0
7	12223	23	3	39	0	55	0
8	7752	24	7	40	0	56	0
9	3788	25	1	41	0	57	0
10	2490	26	5	42	0	58	0
11	1706	27	1	43	0	59	0
12	1095	28	1	44	0	60	0
13	743	29	0	45	0	61	0
14	384	30	0	46	0	62	0
15	105	31	0	47	0	63	0
16	138	32	0	48	0	64	0

TYPED PAGE - WHITE - RIT3/2* - 02 NOVEMBER 1976 - MODE 11

1	162144	17	2127	33	147	49	159
2	39792	18	1688	34	138	50	124
3	53704	19	1765	35	314	51	147
4	33987	20	1352	36	309	52	104
5	17207	21	1308	37	373	53	172
6	15812	22	1120	38	199	54	95
7	16281	23	1064	39	196	55	100
8	3596	24	702	40	251	56	73
9	3614	25	377	41	244	57	92
10	5833	26	729	42	207	58	70
11	6041	27	777	43	232	59	59
12	3554	28	586	44	183	60	73
13	4230	29	567	45	314	61	100
14	2831	30	491	46	171	62	56
15	2726	31	595	47	231	63	58
16	2158	32	455	48	140	64	1201

TYPED PAGE - WHITE - RIT3/2* - 02 NOVEMBER 1976 - MODE 12

1	132542	17	351	33	108	49	13
2	61883	18	594	34	37	50	10
3	45331	19	650	35	70	51	11
4	31546	20	367	36	55	52	7
5	16814	21	371	37	73	53	15
6	9510	22	365	38	35	54	10
7	3132	23	373	39	44	55	5
8	5196	24	376	40	34	56	5
9	5399	25	332	41	33	57	5
10	3305	26	393	42	15	58	1
11	3824	27	291	43	34	59	5
12	2089	28	195	44	14	60	2
13	2080	29	192	45	18	61	3
14	1279	30	158	46	10	62	2
15	1347	31	139	47	13	63	7
16	981	32	103	48	15	64	112

TYPED PAGE - WHITE - RIT3/2* - 02 NOVEMBER 1976 - MODE 13

1	33295	17	342	33	127	49	7
2	26829	18	365	34	110	50	10
3	19698	19	367	35	34	51	11
4	11521	20	411	36	50	52	3
5	10210	21	190	37	44	53	1
6	7250	22	154	38	52	54	12
7	5849	23	111	39	42	55	3
8	4618	24	170	40	40	56	3
9	3888	25	179	41	36	57	7
10	2952	26	209	42	14	58	5
11	2787	27	115	43	13	59	7
12	2145	28	112	44	14	60	7
13	1897	29	198	45	11	61	3
14	1413	30	172	46	12	62	1
15	1288	31	144	47	16	63	3
16	360	32	124	48	17	64	266

TYPED PAGE - WHITE - RIT3/2* - 02 NOVEMBER 1976 - MODE 14

1	55640	17	184	33	157	49	157
2	18841	18	146	34	147	50	35
3	31530	19	433	35	153	51	39
4	3721	20	153	36	198	52	38
5	3989	21	126	37	147	53	30
6	3714	22	130	38	131	54	136
7	4147	23	177	39	170	55	39
8	2462	24	190	40	154	56	30
9	2728	25	190	41	143	57	109
10	1894	26	182	42	153	58	35
11	2155	27	140	43	171	59	75
12	1108	28	131	44	183	60	36
13	1345	29	188	45	135	61	79
14	542	30	149	46	134	62	105
15	790	31	179	47	111	63	37
16	372	32	131	48	130	64	55310

TYPED PAGE - WHITE - *IT3/2* - 02 NOVEMBER 1976 - MODE 15

1	346	17	1156	33	425	49	128
2	356	18	376	34	372	50	122
3	1277	19	525	35	384	51	130
4	1810	20	435	36	1308	52	145
5	1725	21	345	37	289	53	104
6	2839	22	227	38	239	54	131
7	3233	23	190	39	185	55	108
8	2439	24	148	40	174	56	124
9	2337	25	154	41	193	57	109
10	2358	26	153	42	165	58	137
11	2281	27	344	43	36	59	124
12	2203	28	533	44	169	60	59
13	1940	29	577	45	71	61	55
14	1800	30	479	46	30	62	33
15	1649	31	457	47	100	63	30
16	1387	32	440	48	155	64	14961

TYPED PAGE - WHITE - *IT3/2* - 02 NOVEMBER 1976 - MODE 16

1	283921	17	2467	33	177	49	160
2	38909	18	1476	34	120	50	38
3	62747	19	1762	35	435	51	147
4	34671	20	1273	36	149	52	104
5	29855	21	1446	37	131	53	71
6	15686	22	1016	38	107	54	77
7	15722	23	1088	39	159	55	36
8	3633	24	332	40	124	56	58
9	9036	25	1020	41	118	57	73
10	5840	26	571	42	135	58	52
11	5970	27	354	43	105	59	72
12	4115	28	575	44	137	60	61
13	3991	29	624	45	145	61	61
14	2615	30	457	46	120	62	41
15	2811	31	573	47	172	63	54
16	1925	32	366	48	147	64	742

TYPED PAGE - WHITE - *IT3/2* - 02 NOVEMBER 1976 - MODE 11

1	131994	17	776	33	187	49	129
2	37414	18	416	34	227	50	126
3	23106	19	577	35	215	51	108
4	12231	20	410	36	167	52	116
5	9459	21	465	37	109	53	122
6	5757	22	377	38	133	54	110
7	5629	23	558	39	131	55	119
8	3746	24	542	40	117	56	36
9	3708	25	619	41	118	57	112
10	2699	26	569	42	92	58	74
11	2553	27	584	43	95	59	94
12	1693	28	495	44	101	60	55
13	1656	29	446	45	113	61	31
14	1055	30	401	46	95	62	78
15	1084	31	372	47	108	63	64
16	576	32	319	48	122	64	1092

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1	150451	17	1572	33	651	49	323
2	35750	18	1693	34	482	50	198
3	29523	19	1220	35	536	51	193
4	15082	20	342	36	411	52	133
5	14422	21	310	37	416	53	169
6	3597	22	680	38	300	54	203
7	2970	23	679	39	341	55	176
8	6476	24	633	40	299	56	209
9	5778	25	1085	41	341	57	206
10	4692	26	1180	42	231	58	148
11	5108	27	1039	43	261	59	253
12	3373	28	336	44	172	60	149
13	3475	29	368	45	323	61	235
14	2688	30	798	46	274	62	114
15	2254	31	355	47	394	63	183
16	1681	32	657	48	245	64	19235

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1	19395	17	1	33	0	49	0
2	22933	18	0	34	0	50	0
3	6181	19	1	35	0	51	0
4	2937	20	1	36	0	52	0
5	3641	21	0	37	0	53	0
6	1766	22	0	38	0	54	0
7	1501	23	1	39	0	55	0
8	1281	24	0	40	0	56	0
9	1091	25	1	41	0	57	0
10	569	26	0	42	0	58	0
11	504	27	0	43	0	59	0
12	394	28	0	44	0	60	0
13	134	29	0	45	0	61	0
14	30	30	0	46	0	62	0
15	32	31	0	47	0	63	0
16	11	32	0	48	1	64	5

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1	34459	17	184	33	157	49	157
2	11313	18	346	34	147	50	35
3	10892	19	433	35	153	51	39
4	1002	20	263	36	198	52	38
5	3173	21	326	37	147	53	30
6	1592	22	130	38	131	54	136
7	3099	23	277	39	170	55	39
8	1545	24	190	40	154	56	30
9	1324	25	200	41	143	57	109
10	397	26	182	42	153	58	35
11	1363	27	140	43	171	59	76
12	739	28	181	44	203	60	36
13	1030	29	188	45	135	61	79
14	568	30	149	46	134	62	105
15	759	31	179	47	111	63	37
16	369	32	181	48	130	64	35310

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1	1181	17	0	33	0	49	0
2	7528	18	0	34	0	50	0
3	20638	19	0	35	0	51	0
4	4719	20	0	36	0	52	0
5	1816	21	0	37	0	53	0
6	1122	22	0	38	0	54	0
7	1048	23	0	39	0	55	0
8	917	24	0	40	0	56	0
9	304	25	0	41	0	57	0
10	397	26	0	42	0	58	0
11	792	27	0	43	0	59	0
12	309	28	0	44	0	60	0
13	315	29	0	45	0	61	0
14	74	30	0	46	0	62	0
15	21	31	0	47	0	63	0
16	3	32	0	48	0	64	0

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1	346103	17	390	33	110	49	46
2	35140	18	391	34	39	50	47
3	61001	19	308	35	36	51	33
4	16631	20	416	36	101	52	36
5	13477	21	436	37	114	53	35
6	10210	22	139	38	38	54	35
7	3841	23	199	39	35	55	36
8	3956	24	179	40	53	56	31
9	4645	25	130	41	53	57	30
10	1493	26	138	42	71	58	39
11	1557	27	129	43	59	59	39
12	1952	28	191	44	59	60	33
13	1776	29	208	45	55	61	31
14	1032	30	182	46	44	62	33
15	1052	31	108	47	73	63	18
16	779	32	122	48	76	64	282

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1	113955	17	1273	33	310	49	383
2	43801	18	701	34	339	50	212
3	28434	19	1147	35	360	51	239
4	14188	20	591	36	382	52	157
5	10334	21	347	37	384	53	277
6	5276	22	478	38	254	54	154
7	6693	23	709	39	359	55	201
8	2718	24	459	40	325	56	164
9	4328	25	568	41	351	57	276
10	1788	26	359	42	182	58	148
11	2068	27	605	43	316	59	180
12	1012	28	660	44	174	60	123
13	1786	29	581	45	302	61	199
14	370	30	401	46	157	62	137
15	1185	31	559	47	348	63	176
16	701	32	375	48	315	64	19218

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1	135217	17	324	33	10	49	10
2	19431	18	101	34	13	50	7
3	34294	19	302	35	15	51	5
4	16526	20	119	36	13	52	3
5	12099	21	155	37	13	53	11
6	3027	22	35	38	7	54	3
7	5712	23	125	39	15	55	7
8	2470	24	71	40	10	56	1
9	2892	25	39	41	17	57	1
10	1505	26	30	42	10	58	1
11	1944	27	34	43	10	59	5
12	331	28	45	44	3	60	1
13	786	29	41	45	13	61	5
14	399	30	34	46	3	62	1
15	553	31	45	47	3	63	7
16	319	32	25	48	3	64	154

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1	16965	17	329	33	399	49	101
2	3007	18	543	34	415	50	161
3	3549	19	412	35	399	51	156
4	3382	20	335	36	1141	52	137
5	3438	21	384	37	391	53	117
6	3196	22	355	38	392	54	113
7	3697	23	328	39	161	55	98
8	3841	24	369	40	303	56	151
9	3565	25	390	41	307	57	136
10	3629	26	500	42	303	58	101
11	3380	27	524	43	142	59	92
12	3056	28	534	44	120	60	59
13	1932	29	498	45	56	61	70
14	1551	30	513	46	112	62	34
15	1380	31	499	47	157	63	75
16	1041	32	419	48	144	64	13963

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1	54634	17	1764	33	141	49	45
2	10075	18	1136	34	162	50	37
3	3173	19	1334	35	134	51	53
4	2946	20	330	36	147	52	43
5	2007	21	334	37	128	53	53
6	1813	22	741	38	120	54	73
7	1404	23	318	39	132	55	39
8	1593	24	198	40	173	56	51
9	1084	25	181	41	129	57	103
10	1237	26	153	42	117	58	38
11	1763	27	165	43	109	59	106
12	1239	28	112	44	75	60	31
13	1636	29	115	45	54	61	34
14	1126	30	34	46	51	62	39
15	1817	31	114	47	53	63	36
16	1394	32	34	48	55	64	1339

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1	346	17	1156	33	425	49	128
2	356	18	376	34	372	50	122
3	1277	19	325	35	384	51	130
4	1810	20	435	36	1308	52	145
5	1725	21	345	37	189	53	104
6	2839	22	227	38	139	54	131
7	3233	23	190	39	185	55	108
8	2439	24	148	40	174	56	124
9	2337	25	154	41	193	57	109
10	2358	26	153	42	165	58	137
11	2281	27	344	43	36	59	124
12	2203	28	333	44	169	60	59
13	1940	29	377	45	71	61	55
14	1800	30	479	46	30	62	33
15	1649	31	457	47	100	63	30
16	1387	32	440	48	155	64	14961

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1	504183	17	566	33	68	49	14
2	151993	18	436	34	79	50	32
3	34208	19	399	35	55	51	18
4	40191	20	408	36	56	52	14
5	25633	21	218	37	51	53	17
6	13859	22	308	38	35	54	15
7	3961	23	213	39	36	55	3
8	5909	24	167	40	25	56	3
9	4753	25	137	41	27	57	7
10	2903	26	138	42	40	58	11
11	2707	27	112	43	27	59	7
12	1542	28	114	44	22	60	4
13	1323	29	113	45	18	61	5
14	923	30	32	46	22	62	12
15	371	31	36	47	9	63	7
16	602	32	65	48	11	64	72

IEEE FACS CHART - NO FILTER - BIT9/2% - 03 NOVEMBER 1976 - MODE 1

1	369348	17	1232	33	348	49	130
2	29578	18	782	34	234	50	104
3	57435	19	377	35	183	51	39
4	26124	20	304	36	236	52	110
5	20830	21	359	37	227	53	35
6	9136	22	492	38	192	54	58
7	10050	23	518	39	270	55	78
8	5111	24	399	40	204	56	75
9	5151	25	491	41	215	57	59
10	2629	26	313	42	154	58	52
11	3830	27	453	43	156	59	59
12	2011	28	298	44	134	60	41
13	2469	29	420	45	107	61	64
14	1342	30	312	46	115	62	52
15	1671	31	338	47	127	63	34
16	925	32	369	48	124	64	1186

IEEE FACS CHART - NO FILTER - BIT9/2% - 03 NOVEMBER 1976 - MODE 2

1	250986	17	1194	33	458	49	139
2	57676	18	709	34	343	50	106
3	18429	19	1125	35	307	51	135
4	16926	20	302	36	387	52	125
5	13965	21	359	37	296	53	158
6	7041	22	558	38	175	54	120
7	7196	23	762	39	198	55	117
8	3055	24	443	40	135	56	113
9	3963	25	569	41	460	57	133
10	1916	26	489	42	214	58	142
11	2710	27	456	43	301	59	132
12	1270	28	520	44	172	60	95
13	1607	29	511	45	242	61	37
14	1142	30	391	46	113	62	107
15	1473	31	513	47	216	63	136
16	1026	32	382	48	166	64	5498

IEEE FACS CHART - NO FILTER - *IT9/2* - 03 NOVEMBER 1976 - MODE 3

1	165315	17	672	33	192	49	79
2	46455	18	789	34	149	50	95
3	30198	19	594	35	159	51	58
4	18040	20	310	36	129	52	41
5	7973	21	332	37	122	53	47
6	3967	22	180	38	95	54	40
7	3481	23	168	39	104	55	30
8	1973	24	218	40	107	56	42
9	1537	25	272	41	126	57	45
10	1102	26	213	42	130	58	38
11	1103	27	229	43	115	59	31
12	392	28	213	44	73	60	27
13	355	29	251	45	115	61	52
14	488	30	185	46	56	62	33
15	473	31	192	47	33	63	31
16	448	32	187	48	155	64	2389

IEEE FACS CHART - NO FILTER - *IT9/2* - 03 NOVEMBER 1976 - MODE 4

1	57002	17	2712	33	366	49	103
2	34177	18	3943	34	377	50	333
3	35271	19	1629	35	156	51	142
4	11147	20	720	36	471	52	162
5	3618	21	251	37	502	53	136
6	5173	22	1463	38	326	54	156
7	5595	23	318	39	400	55	156
8	4488	24	582	40	796	56	131
9	3257	25	496	41	469	57	130
10	2211	26	384	42	270	58	109
11	2337	27	502	43	398	59	105
12	2438	28	440	44	746	60	111
13	2353	29	493	45	304	61	132
14	1543	30	444	46	291	62	114
15	1345	31	532	47	324	63	95
16	979	32	516	48	370	64	27506

IEEE FACS CHART - NO FILTER - KIT9/2* - 03 NOVEMBER 1976 - MODE 5

1	3370	17	315	33	77	49	51
2	11704	18	177	34	33	50	14
3	23218	19	142	35	45	51	15
4	10369	20	202	36	73	52	53
5	11756	21	1109	37	79	53	157
6	3285	22	1003	38	34	54	55
7	2115	23	133	39	199	55	30
8	2284	24	54	40	381	56	59
9	1182	25	32	41	190	57	36
10	1070	26	34	42	30	58	31
11	770	27	47	43	58	59	52
12	747	28	124	44	53	60	37
13	545	29	197	45	52	61	32
14	575	30	423	46	20	62	22
15	404	31	121	47	43	63	14
16	360	32	37	48	24	64	14471

IEEE FACS CHART - NO FILTER - KIT9/2* - 03 NOVEMBER 1976 - MODE 6

1	491545	17	517	33	38	49	10
2	158458	18	396	34	46	50	14
3	36545	19	394	35	19	51	5
4	41392	20	311	36	35	52	13
5	17614	21	232	37	45	53	1
6	13834	22	197	38	51	54	1
7	10000	23	187	39	59	55	1
8	5382	24	133	40	74	56	2
9	4828	25	91	41	37	57	2
10	2963	26	106	42	38	58	11
11	2835	27	58	43	12	59	3
12	1472	28	50	44	18	60	1
13	1218	29	41	45	37	61	2
14	993	30	56	46	12	62	3
15	1041	31	38	47	16	63	2
16	553	32	41	48	9	64	56

IEEE FACS CHART - NO FILTER - BIT9/2% - 03 NOVEMBER 1976 - MODE 11

1	360728	17	1367	33	336	49	119
2	99606	18	931	34	168	50	31
3	68149	19	1059	35	194	51	107
4	36747	20	568	36	155	52	120
5	21753	21	941	37	225	53	136
6	11593	22	622	38	118	54	76
7	10481	23	650	39	165	55	30
8	5661	24	499	40	124	56	73
9	6145	25	426	41	190	57	63
10	3557	26	356	42	154	58	40
11	3604	27	379	43	177	59	75
12	2507	28	308	44	104	60	57
13	2600	29	335	45	142	61	64
14	1608	30	241	46	92	62	38
15	2092	31	297	47	127	63	52
16	1143	32	234	48	34	64	1518

IEEE FACS CHART - NO FILTER - BIT9/2% - 03 NOVEMBER 1976 - MODE 12

1	145014	17	1640	33	549	49	32
2	33585	18	364	34	401	50	108
3	45734	19	333	35	173	51	115
4	19259	20	535	36	146	52	37
5	15357	21	543	37	164	53	113
6	7367	22	483	38	251	54	106
7	7711	23	587	39	216	55	110
8	5145	24	334	40	134	56	105
9	3721	25	429	41	113	57	150
10	2105	26	375	42	120	58	105
11	2784	27	461	43	131	59	106
12	1700	28	329	44	168	60	100
13	1929	29	416	45	166	61	30
14	1906	30	331	46	112	62	34
15	2275	31	342	47	127	63	34
16	1649	32	254	48	142	64	5472

IEEE FACS CHART - NO FILTER - KIT9/2* - 03 NOVEMBER 1976 - MODE 13

1	138884	17	2156	33	542	49	245
2	29985	18	2030	34	532	50	138
3	28451	19	1662	35	494	51	173
4	18919	20	1663	36	419	52	161
5	12743	21	1478	37	307	53	208
6	7359	22	513	38	314	54	243
7	7024	23	317	39	305	55	281
8	3746	24	462	40	400	56	148
9	4387	25	786	41	531	57	192
10	3087	26	479	42	307	58	154
11	3880	27	503	43	208	59	245
12	2414	28	564	44	272	60	140
13	2534	29	514	45	270	61	218
14	2056	30	419	46	234	62	138
15	1598	31	525	47	231	63	152
16	2146	32	400	48	222	64	17712

IEEE FACS CHART - NO FILTER - KIT9/2* - 03 NOVEMBER 1976 - MODE 14

1	124605	17	101	33	32	49	33
2	38063	18	130	34	138	50	43
3	39659	19	157	35	73	51	36
4	7890	20	100	36	106	52	42
5	3364	21	130	37	123	53	30
6	1325	22	37	38	110	54	39
7	1712	23	120	39	71	55	40
8	1129	24	75	40	138	56	30
9	314	25	36	41	138	57	46
10	556	26	53	42	39	58	43
11	564	27	129	43	35	59	49
12	423	28	157	44	--	60	40
13	608	29	133	45	34	61	43
14	195	30	190	46	75	62	53
15	388	31	125	47	104	63	33
16	165	32	39	48	51	64	3434

IEEE FACS CHART - NO FILTER - KIT9/2* - 03 NOVEMBER 1976 - MODE 15

1	10293	17	4036	33	319	49	131
2	13745	18	3886	34	105	50	130
3	15903	19	1799	35	138	51	134
4	5518	20	583	36	382	52	329
5	4130	21	708	37	341	53	174
6	2900	22	1271	38	334	54	107
7	3010	23	594	39	361	55	104
8	2389	24	395	40	775	56	140
9	1970	25	329	41	337	57	392
10	1446	26	242	42	148	58	75
11	1254	27	365	43	319	59	47
12	1752	28	352	44	373	60	57
13	380	29	365	45	1086	61	37
14	1123	30	358	46	192	62	77
15	321	31	490	47	177	63	51
16	391	32	393	48	325	64	19205

IEEE FACS CHART - NO FILTER - KIT9/2* - 03 NOVEMBER 1976 - MODE 16

1	364730	17	1583	33	185	49	38
2	39339	18	390	34	136	50	70
3	66848	19	1082	35	171	51	38
4	27132	20	735	36	132	52	71
5	20687	21	316	37	131	53	101
6	10452	22	548	38	149	54	60
7	3973	23	553	39	120	55	71
8	5228	24	459	40	131	56	36
9	5476	25	564	41	169	57	72
10	3170	26	406	42	118	58	55
11	3681	27	524	43	197	59	70
12	2648	28	402	44	106	60	45
13	2419	29	437	45	159	61	37
14	1596	30	391	46	32	62	55
15	1898	31	319	47	118	63	32
16	1059	32	325	48	32	64	1942

IEEE FACS CHART - NO FILTER - KIT3/2* - 03 NOVEMBER 1976 - MODE 11

1	254601	17	1264	33	355	49	358
2	74008	18	311	34	402	50	139
3	44211	19	1273	35	355	51	123
4	15080	20	396	36	401	52	30
5	11688	21	343	37	534	53	149
6	5688	22	458	38	309	54	24
7	5582	23	387	39	233	55	127
8	3884	24	368	40	300	56	59
9	3284	25	430	41	341	57	128
10	1905	26	344	42	359	58	110
11	2440	27	364	43	242	59	180
12	1838	28	319	44	306	60	76
13	2631	29	337	45	187	61	133
14	2045	30	356	46	169	62	58
15	1574	31	373	47	113	63	33
16	1284	32	503	48	146	64	7435

IEEE FACS CHART - NO FILTER - KIT3/2* - 03 NOVEMBER 1976 - MODE 12

1	124904	17	1026	33	406	49	79
2	52406	18	381	34	565	50	109
3	44472	19	399	35	516	51	107
4	16914	20	522	36	432	52	140
5	10407	21	503	37	328	53	124
6	6954	22	446	38	377	54	75
7	5143	23	413	39	379	55	112
8	2922	24	387	40	158	56	90
9	2125	25	247	41	288	57	113
10	1703	26	170	42	317	58	39
11	1544	27	292	43	561	59	106
12	1150	28	201	44	190	60	78
13	1412	29	258	45	142	61	50
14	1684	30	231	46	120	62	53
15	3294	31	357	47	123	63	77
16	1377	32	517	48	126	64	3788

IEEE FACS CHART - NO FILTER - KIT9/2* - 03 NOVEMBER 1976 - MODE 23

1	114029	17	144	33	39	49	32
2	40877	18	183	34	182	50	74
3	17165	19	379	35	190	51	125
4	16920	20	1471	36	126	52	41
5	5857	21	135	37	120	53	44
6	2743	22	138	38	33	54	45
7	2588	23	221	39	35	55	39
8	1417	24	73	40	100	56	34
9	1229	25	97	41	268	57	39
10	390	26	111	42	122	58	21
11	385	27	77	43	176	59	53
12	506	28	70	44	34	60	35
13	500	29	36	45	38	61	37
14	392	30	52	46	30	62	31
15	315	31	114	47	73	63	39
16	220	32	37	48	29	64	3821

IEEE FACS CHART - NO FILTER - KIT9/2* - 03 NOVEMBER 1976 - MODE 24

1	54925	17	226	33	30	49	19
2	19505	18	1131	34	100	50	26
3	18336	19	1206	35	53	51	19
4	5560	20	141	36	39	52	21
5	3174	21	188	37	134	53	27
6	1726	22	134	38	71	54	26
7	1905	23	110	39	71	55	24
8	770	24	35	40	48	56	31
9	371	25	103	41	42	57	19
10	439	26	73	42	35	58	23
11	739	27	208	43	41	59	17
12	416	28	180	44	49	60	19
13	1437	29	168	45	43	61	15
14	404	30	180	46	32	62	21
15	358	31	225	47	39	63	22
16	168	32	214	48	47	64	6569

IEEE FACS CHART - NO FILTER - BIT9/2* - 03 NOVEMBER 1976 - MODE 15

1	3370	17	315	33	77	49	51
2	11704	18	177	34	33	50	24
3	23218	19	142	35	45	51	25
4	10369	20	302	36	33	52	33
5	11756	21	1109	37	78	53	157
6	3285	22	1003	38	34	54	55
7	2115	23	133	39	199	55	30
8	2284	24	54	40	381	56	59
9	1182	25	32	41	190	57	26
10	1070	26	34	42	30	58	31
11	770	27	47	43	58	59	52
12	747	28	124	44	53	60	37
13	545	29	497	45	52	61	32
14	575	30	423	46	20	62	22
15	404	31	121	47	43	63	44
16	360	32	37	48	24	64	14471

IEEE FACS CHART - NO FILTER - BIT9/2* - 03 NOVEMBER 1976 - MODE 16

1	365601	17	1200	33	272	49	116
2	100542	18	397	34	233	50	99
3	56165	19	387	35	217	51	131
4	28234	20	362	36	226	52	111
5	20570	21	306	37	161	53	149
6	10396	22	385	38	178	54	45
7	3969	23	353	39	152	55	57
8	5518	24	461	40	171	56	55
9	4885	25	301	41	154	57	59
10	3654	26	372	42	171	58	59
11	3316	27	439	43	130	59	53
12	1956	28	276	44	146	60	32
13	2445	29	355	45	90	61	49
14	1670	30	230	46	109	62	21
15	1699	31	265	47	93	63	48
16	1559	32	229	48	128	64	119

IEEE FACS CHART - NO FILTER - *IT9/2* - 03 NOVEMBER 1976 - MODE 31

1	240995	17	1434	33	239	49	124
2	71544	18	1141	34	240	50	129
3	48428	19	342	35	270	51	127
4	18957	20	490	36	480	52	123
5	14697	21	579	37	375	53	177
6	3725	22	393	38	458	54	114
7	3747	23	498	39	214	55	170
8	3965	24	562	40	148	56	119
9	4452	25	411	41	204	57	94
10	2713	26	290	42	209	58	78
11	2241	27	437	43	180	59	96
12	1786	28	257	44	173	60	31
13	1944	29	442	45	171	61	76
14	1093	30	311	46	188	62	35
15	1521	31	390	47	199	63	35
16	1190	32	365	48	122	64	5276

IEEE FACS CHART - NO FILTER - *IT9/2* - 03 NOVEMBER 1976 - MODE 32

1	152691	17	1349	33	465	49	258
2	50568	18	736	34	279	50	246
3	28201	19	726	35	271	51	221
4	11298	20	583	36	185	52	355
5	3120	21	335	37	240	53	189
6	4850	22	1267	38	229	54	33
7	1440	23	540	39	261	55	37
8	2801	24	564	40	154	56	30
9	2334	25	384	41	320	57	121
10	1714	26	385	42	330	58	105
11	1789	27	462	43	248	59	147
12	1431	28	282	44	347	60	77
13	1165	29	725	45	258	61	124
14	1224	30	393	46	200	62	59
15	1005	31	359	47	224	63	30
16	1092	32	330	48	131	64	10985

IEEE FACS CHART - NO FILTER - *IT9/2* - 03 NOVEMBER 1976 - MODE 33

1	60202	17	2475	33	568	49	240
2	39748	18	399	34	144	50	150
3	32869	19	2011	35	334	51	248
4	18148	20	2385	36	511	52	133
5	3941	21	1089	37	504	53	203
6	1432	22	380	38	336	54	185
7	4827	23	535	39	1042	55	354
8	2713	24	309	40	438	56	166
9	3345	25	529	41	417	57	152
10	1754	26	324	42	294	58	77
11	2049	27	465	43	357	59	158
12	1674	28	1057	44	242	60	157
13	1572	29	572	45	564	61	134
14	1034	30	410	46	144	62	116
15	1606	31	484	47	310	63	133
16	1460	32	473	48	191	64	21737

IEEE FACS CHART - NO FILTER - *IT9/2* - 03 NOVEMBER 1976 - MODE 34

1	32711	17	1303	33	276	49	193
2	3958	18	511	34	257	50	246
3	19151	19	1148	35	142	51	240
4	7532	20	754	36	366	52	170
5	14851	21	1617	37	327	53	226
6	5394	22	1167	38	337	54	229
7	3947	23	560	39	405	55	136
8	2885	24	297	40	539	56	112
9	3146	25	461	41	336	57	202
10	1911	26	411	42	186	58	558
11	2446	27	337	43	217	59	120
12	1376	28	346	44	249	60	124
13	1650	29	380	45	198	61	132
14	1303	30	299	46	312	62	39
15	1336	31	328	47	259	63	155
16	342	32	277	48	233	64	28140

IEEE FACS CHART - NO FILTER - KIT9/2* - 03 NOVEMBER 1976 - MODE 35

1	10293	17	1036	33	219	49	181
2	13745	18	3886	34	205	50	330
3	15903	19	1799	35	188	51	184
4	5518	20	583	36	382	52	329
5	4130	21	708	37	341	53	274
6	2900	22	1271	38	234	54	107
7	3010	23	594	39	361	55	104
8	2389	24	395	40	776	56	140
9	1930	25	329	41	337	57	282
10	1446	26	242	42	148	58	76
11	1254	27	265	43	219	59	17
12	1752	28	252	44	573	60	57
13	380	29	265	45	1096	61	37
14	1123	30	258	46	292	62	7
15	321	31	190	47	277	63	51
16	391	32	283	48	326	64	19205

IEEE FACS CHART - NO FILTER - KIT9/2* - 03 NOVEMBER 1976 - MODE 36

APPENDIX E: IMAGE ENHANCEMENT

Prepared

for

US POSTAL SERVICE

October 1976

by

Frank C Martin

NAVAL ELECTRONICS LABORATORY CENTER

San Diego, CA

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NONRECURSIVE FILTER CALCULATIONS . . . EA-1

INTRODUCTION

This report is the last in a series of six summary reports due in FY76. The subject covered is image enhancement. The year's efforts in this area were expended in three types of enhancement–edge enhancement, color filtering, and video compression. A discussion of the three types and example images showing the results are presented in the body of the report.

EDGE ENHANCEMENT

Edge enhancement is a technique used in television presentations. It is used to accentuate the perimeters of block letters used in titles, advertisements, and messages presented on the screen. This is accomplished by employing two-dimensional filtering to the message frame. Some discussion and a tentative two-dimensional algorithm were included in the first annual report* on the program. Due to other commitments employing the test bed, the algorithm was not tested until recently.

The derivation of the equation for edge enhancement in one dimension is given in appendix A (to this appendix). A nonrecursive filter was used for the principal investigation in order to preserve symmetry of the effect on both leading and trailing edges of the enhanced area. The equation for the simplest filter, and one which can be fabricated in hardware form to operate in real time at 21 megapels per second is as follows:

$$\frac{E_o}{E_I} = \frac{-K_1 Z^2 + (1 + 2K_1) Z - K_1}{Z^2},$$

where K_1 is a positive fractional constant which can be chosen to vary the amplitude of the enhancement effect.

This equation was used to formulate the two-dimensional equivalent which follows:

S_1	S_2	S_3
S_4	C	S_5
S_6	S_7	S_8

C = brightness amplitude of center pel

$S_1 - S_8$ = brightness amplitude of surrounding pels

Output, $C_E = C(2K + 1) - K$ (S highest + S lowest)

Unless $C \lesssim$ every member of the set S_n, in which case let $C_E = C$

This chosen algorithm does not exactly search the four linear profiles which are: (1) $S_1\ C\ S_8$; (2) $S_2\ C\ S_7$; (3) $S_3\ C\ S_6$; (4) $S_5\ C\ S_4$. The steepest profile should be identified and the linear algorithm should be used to process this profile to find a value C_E for the center pel. In view of the processing complexity required, the chosen algorithm appears to be a good compromise.

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*First Annual Report–Advanced Mail Systems Scanner Technology, NELC Technical Report TR 1995, 22 October 1975, p. 79-85

The algorithm was programmed to operate on portions of images utilizing the frame store memory controller as the processor. Although the processor operates at a relatively high execution rate, it requires about 45 minutes to process a 432 by 440 pel section of an image.

The first image processed contained a set of concentric squares of different brightness. The image area was divided into nine parts (three rows of three columns). Figure E1 shows the results of enhancement on the sets of squares. The software program will accommodate various values of the enhancement constant K from zero to seven-eighths in one-eighth increments. The upper left and lower right portions of Figure E1 are unenhanced (K=0) The chart at the lower left of the figure shows locations and magnitude of the enhancement constants.

The Conrac RQB monitor features a video signal polarity-reversing switch. With this switch the light and dark areas of an image may be transposed. Figure E1 also shows the results of utilizing reversed or inverted video.

The value of the brightness of the background in figure E1 is 00. The brightness of the second square is 20 and the brightness of the small square is 60. In examining the effect of the various enhancement constants in figure E1, it appears that the center image is the most pleasing. For this image the enhancement constant, K, equals 0.5. With a constant K=0.5, the gain of the system is G = 3.0 at the Nyquist limit. It should be noted that this center area of the image also appears most pleasing when the negative video is used for the display. This indicates that the algorithm is working properly for both positive and negative excursions of the video signal.

It should be noted that the centers of the images are a little sharper in photographic focus than the corners due to the curvatures of the CRT face and the camera field. However, the enhancement improvement observed by careful examination of the CRT image is almost as shown in the photograph.

The same set of enhancement constants was employed in presenting a portion of the typed image. The photograph and enhancement constant map are shown on figure E2. Again, a value of K equal to about 0.5 appears to be the best. This particular constant is probably the simplest to accommodate in a real-time hardware implementation.

A second enhancement algorithm was examined and evaluated on the test bed. This algorithm uses the recursive digital filter process to reduce the low-frequency gain with respect to the higher-frequency details of an image. The algorithm was described by Corrington.* We have used the algorithm on the same test data used for the nonrecursive filter. This two-dimensional filter operates line-at-a-time across and then downward as in TV scan.

The dimensions and the coefficients of the matrix were the same as used in Corrington's example. Both the input and output arrays are two by two matrices. The paper states that the technique does not provide symmetry about either the horizontal or vertical axis. This lack of symmetry can be observed in figure E3.

Because it was difficult to predict the enhancement effect which might occur with typed copy, the algorithm was run on a sample typed area. The results are shown in Figure E4. The copy legibility of the enhanced areas is quite good. The time to process the two quadrants for enhancement is approximately 20 minutes in the software/hardware of the frame store memory controller.

---

* Two Dimensional Recursive Digital Filters for Background Removal in Pictures, by Murjan S Corrington, Circuits & Systems Society Newsletter, vol 7, no 6, December 1973

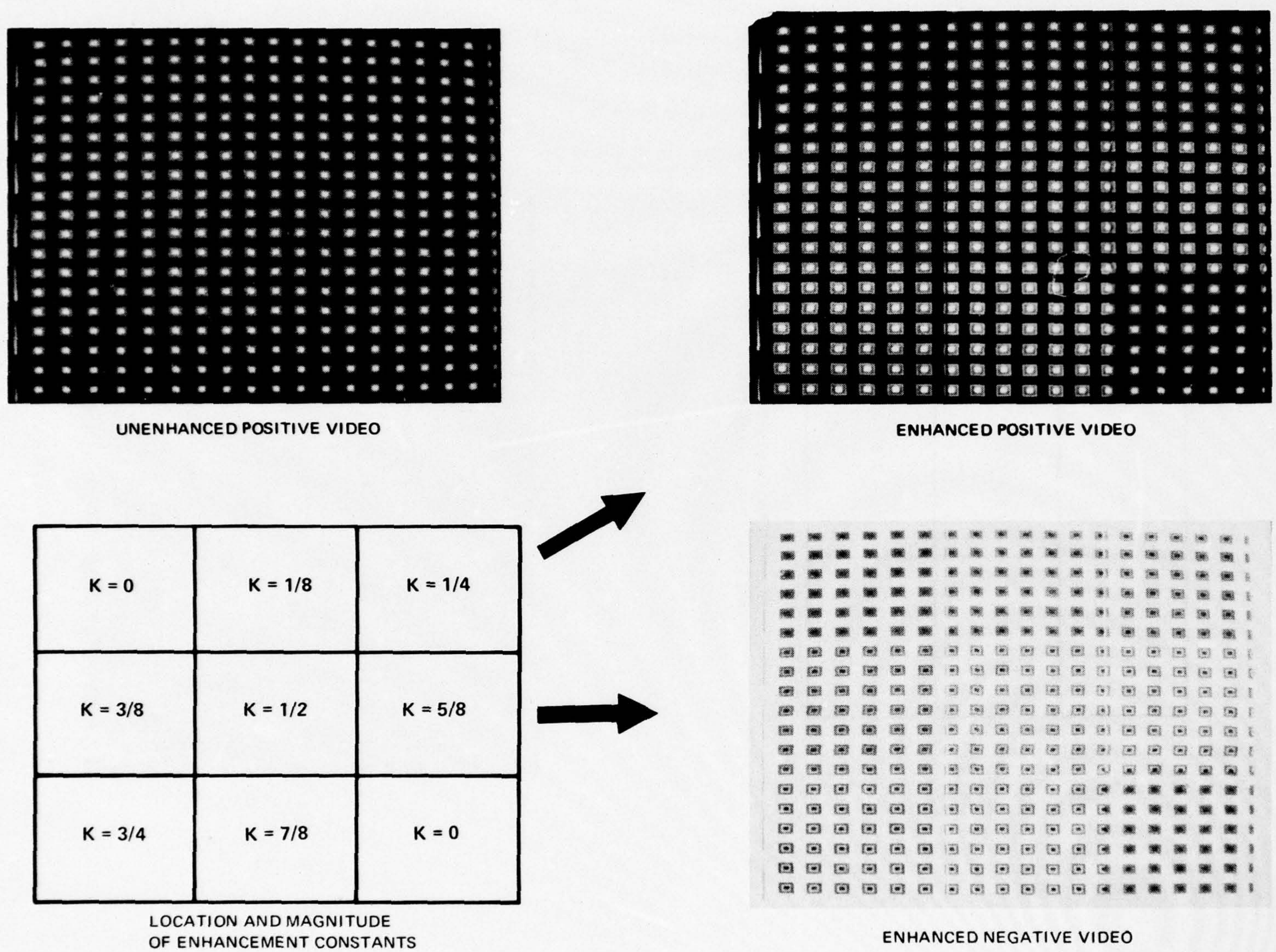
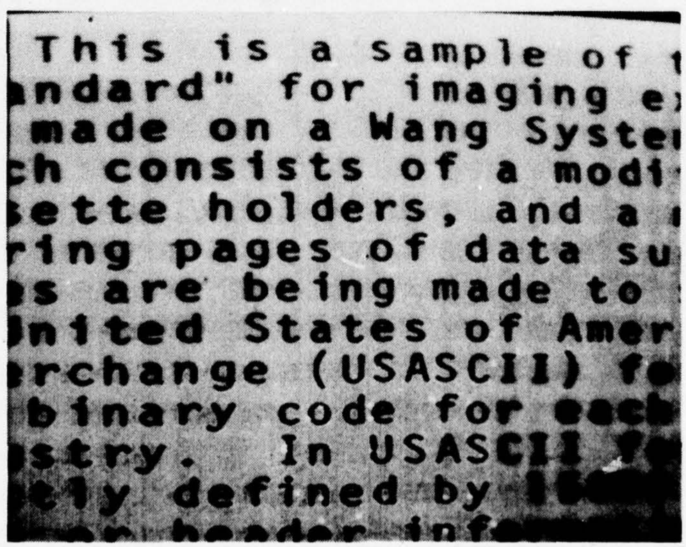


Figure E1. Effects of nonrecursive filter enhancement on test pattern image.

K = 0	K = 1/8	K = 1/4
K = 3/8	K = 1/2	K = 5/8
K = 3/4	K = 7/8	K = 0

LOCATION AND MAGNITUDE
OF ENHANCEMENT CONSTANTS


This is a sample of t
ndard" for imaging e
made on a Wang Syste
ch consists of a modi
ette holders, and a
ring pages of data su
s are being made to
nited States of Amer
rchange (USASCII) f
binary code for eac
stry. In USASCII f
y defined by

ENHANCED POSITIVE VIDEO

Figure E2. Effects of nonrecursive filter enhancement on typed copy image.

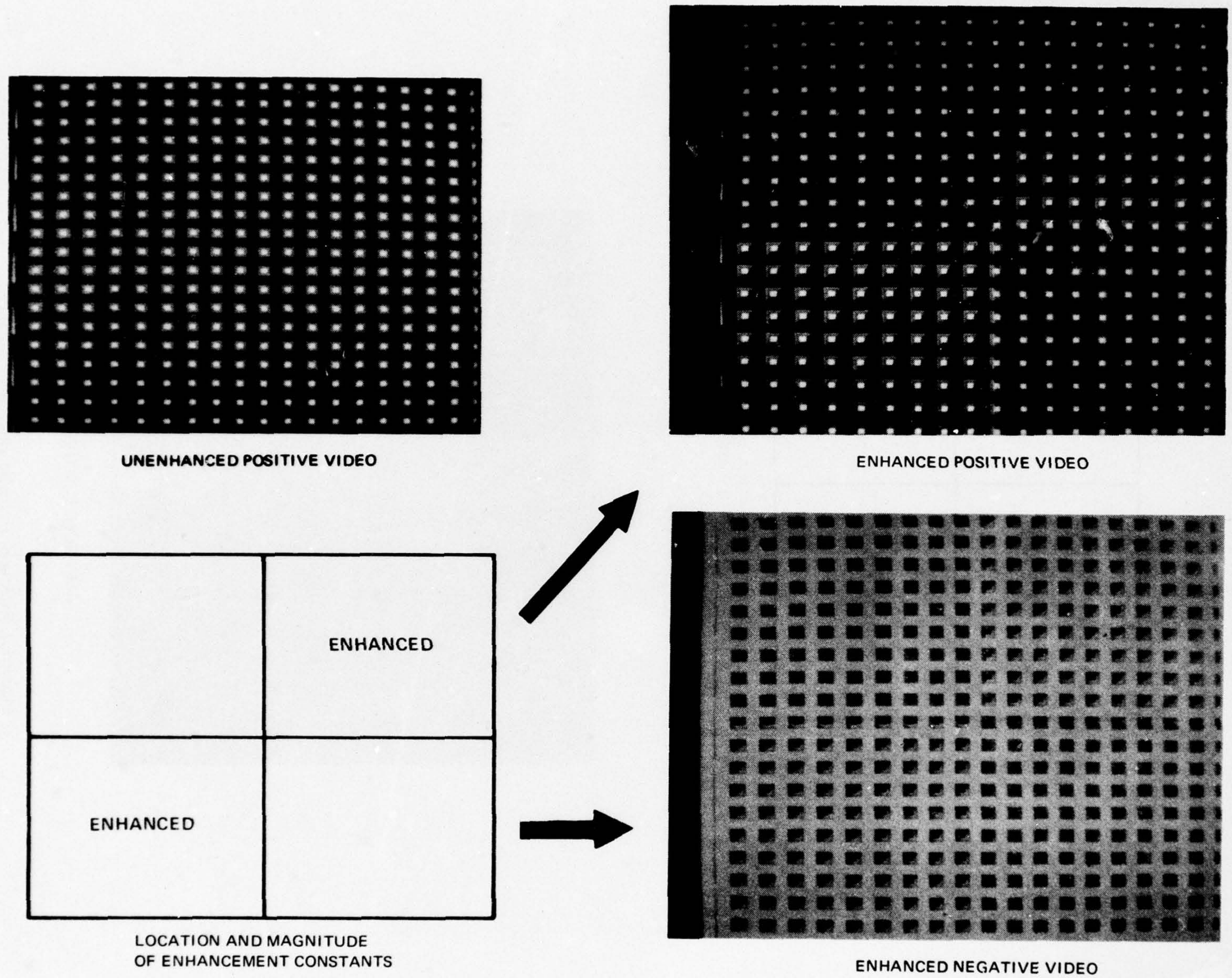
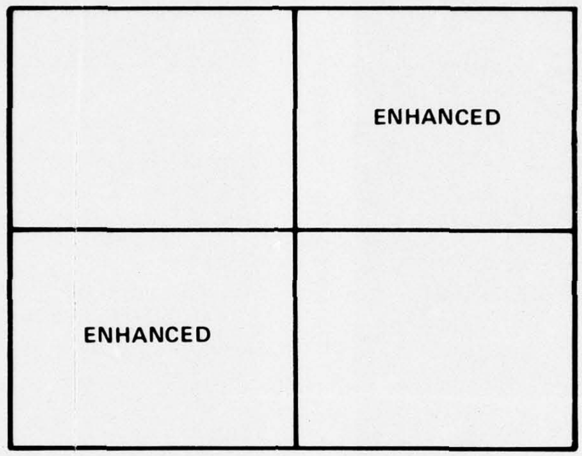
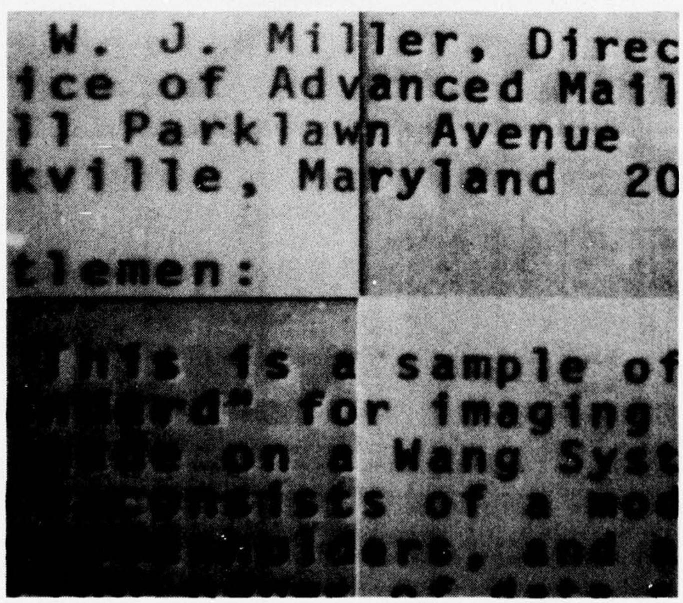


Figure E3. Effects of recursive filter enhancement on test pattern image.



LOCATION OF
ENHANCED AREAS



ENHANCED POSITIVE VIDEO

Figure E4. Effects of recursive filter enhancement.

The complexity of a hardware equivalent of either the recursive or nonrecursive filter is about the same. For real-time processing, high-speed access to the entire data from two previously scanned lines and the present data is necessary. This requires two high-speed memory banks having 1700 six-bit words each, plus the arithmetic logic and control unit, which is nontrivial.

COLOR FILTERING

If colored inks and/or colored paper substrates are used, changes in reflection density can be obtained by the use of color filters placed in the illumination or optical path.

The response of a charge coupled device (CCD) imager is not uniform with respect to frequency of impinging radiation. A CCD has much higher response in the red and near infrared region than in the blue. In order to provide panchromatic system response, the illumination source is designed to produce more spectral energy in the blue and green regions than in the red. Two 18-inch, 30-watt fluorescent tubes are used to illuminate the exposure area of the large drum. The tubes were obtained from GTE Sylvania. A special mixture of phosphors was used in the tubes. The ratio of blue: green: red energy of illumination is about 8:2:1.

Figure E5 shows the relationship of the relative responses of the imager and the illumination sources. Also shown in the figure are the bandwidth of the color separation filter set. A 3-inch gelatine filter holder accommodates the Wratten 47B, 58, or 25 filters and/or neutral density filters.

Often a goal in image acquisition is an increase in print contrast ratio (PCR). PCR is defined as the absolute value of the difference in reflectance of the substrate (background) minus the reflectance of the ink all divided by the background reflectance. Or:

$$PCR = \frac{|R_B - R_I|}{R_B} .$$

By selecting the filter used in imaging, it is possible to enhance the PCR by increasing the relative background reflectance with respect to the ink (or vice versa).

For our experiment a multicolored subscription circular was mounted on the test drum. The image was captured at f16 with white light (no filter) and at wider apertures with each of the three filters.

Figure E6 is a black and white copy of the subject. Colors of the various characters, borders, and backgrounds are noted on the figure. Black, yellow, and dull red inks are used in printing the image.

Comparative photographs of two of the image areas were taken for this report. The first of these is of an area near the top of the image. This area affords clear-cut examples of the ability of color filtering to effect changes in PCR. Figure E7 shows four views of the same portion of the copy. Starting with the image in the upper right which was captured with white light and comparing clockwise with the images captured with red, blue, and green filters, respectively, distinct differences can be seen in the information acquired.

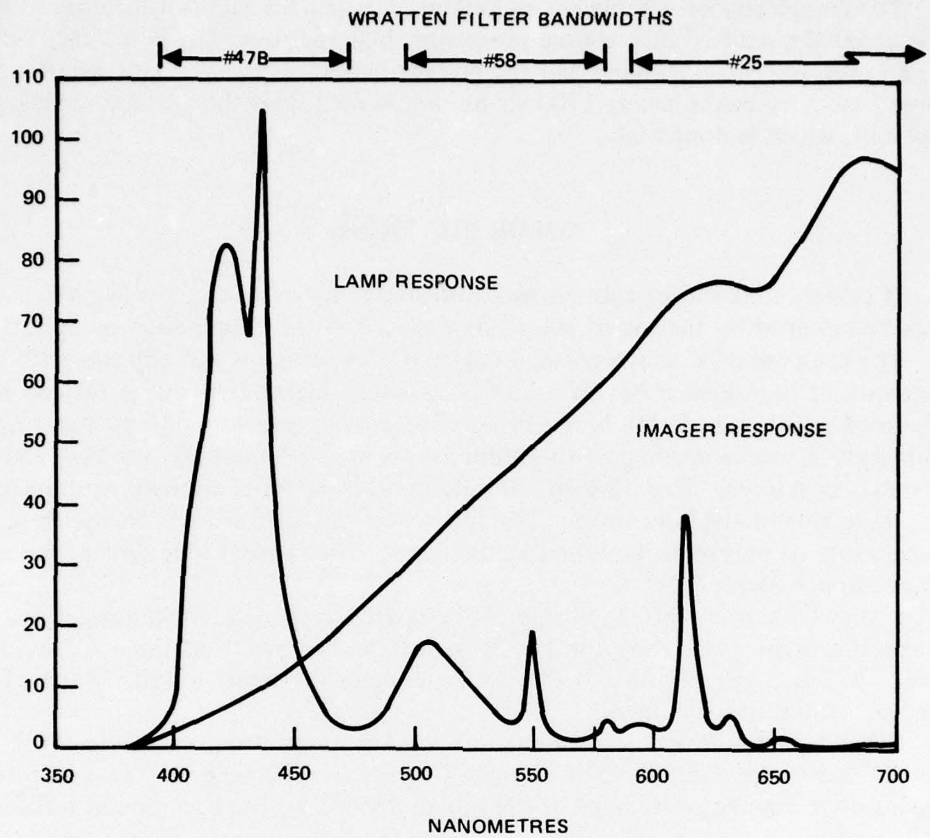


Figure E5. Lamp and imager spectral response.

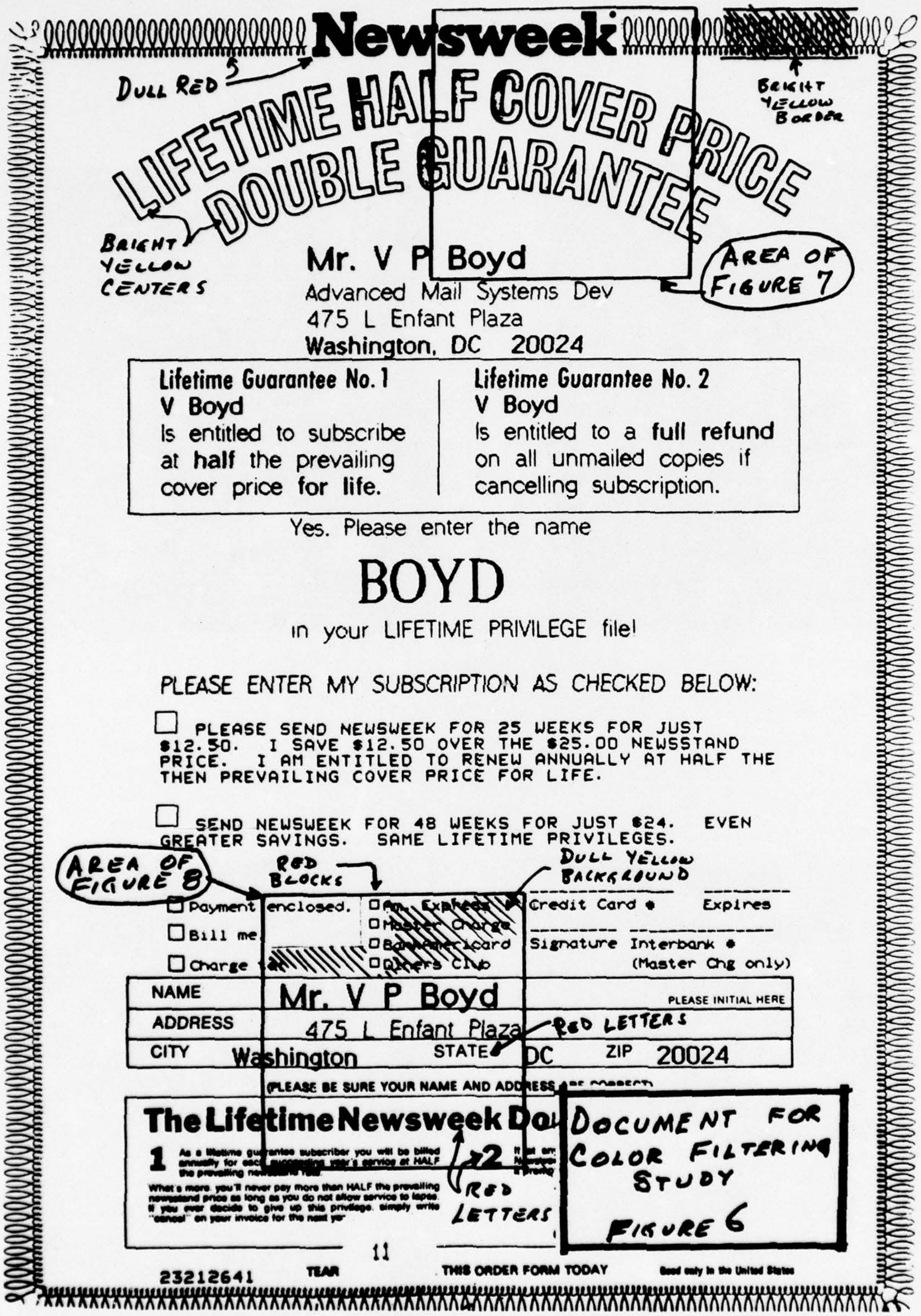

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Figure E6. Document for color filtering study.

Figure E7. Effect of optical filtering on a multicolor document.

In the black and white image and, to a lesser degree, the green image below it, the panchromatic response is noticeable. The word "week" is printed in a dull red color. The scroll design which follows the word "week" is also in dull red ink. The scroll is overlaid on a bright yellow border. The words "cover" and "guarantee" have black borders with yellow printing within the characters.

The choices of contrasts available can be observed by comparing the four images. For selection of high contrast between the red scroll and the yellow background, the green filtered image on the lower left should be selected. For high contrast of the outlines of the words "cover" and "guarantee" with respect to the interior of each letter, the red filtered image in the upper right should be selected. Also, the scroll and its background are completely missing in this image. In the blue image directly below, the high-reflectance spectra of the scroll and its yellow field have been filtered out and that portion of the image turns very dark.

Figure E8 shows another area of the same image, also captured with white light and with the three color filters. The same modification of reflection density by the use of filters is evident in this set of images. As a general rule, the use of a filter having the same spectral passband as the ink or substrate copy of interest will cause that ink or substrate to be acquired as a higher brightness shade. Conversely, the combination of a filter and an ink or substrate at the opposite ends of the spectrum tends to produce a darker brightness level of reflection density.

One of the concerns of the image acqusition process for USPS is the ability to read and authenticate signatures. This is especially true if the originator of a letter or contract document is allowed to use ink of any color. Color filtering can help in enhancing the PCR of a signature if a way can be found to detect the color it is written in. If not, then careful attention must be given to provide a good panchromatic system response. Black ink on white paper appears to have essentially the same PCR regardless of the filtering process. This portion of the imaging study using spectral control of the illumination indicates that color separation filtering for the production of full color images can be accomplished with little difficulty.

LOGARITHMIC VIDEO AMPLITUDE COMPRESSION

One method of reducing the number of bits required to transmit an image with little degradation in visual acceptability is to quantize the video amplitude information in a logarithmic fashion. Conversely, given a fixed number of bits per pel for defining the amplitude, a much enhanced visual image can be defined by using a log compression technique.

There are some problems concerned with log compression. One of these problems is related to the limits of quantization and resolution which can be obtained from analog-to-digital (A/D) converters. There exists a limit to the minimum size of the quantized steps, largely due to system noise and the accuracy and stability of converter threshold circuits. For this reason in log compression it is desirable to utilize the first few A/D converter steps without modification until a point is reached in the sequence at which log steps are equal to or larger than the A/D converter manufacturer's standard step sizes.

At this point, there are two options for log partitioning of the remaining steps. One method is to modify the reference resistor divider string to provide logarithmically

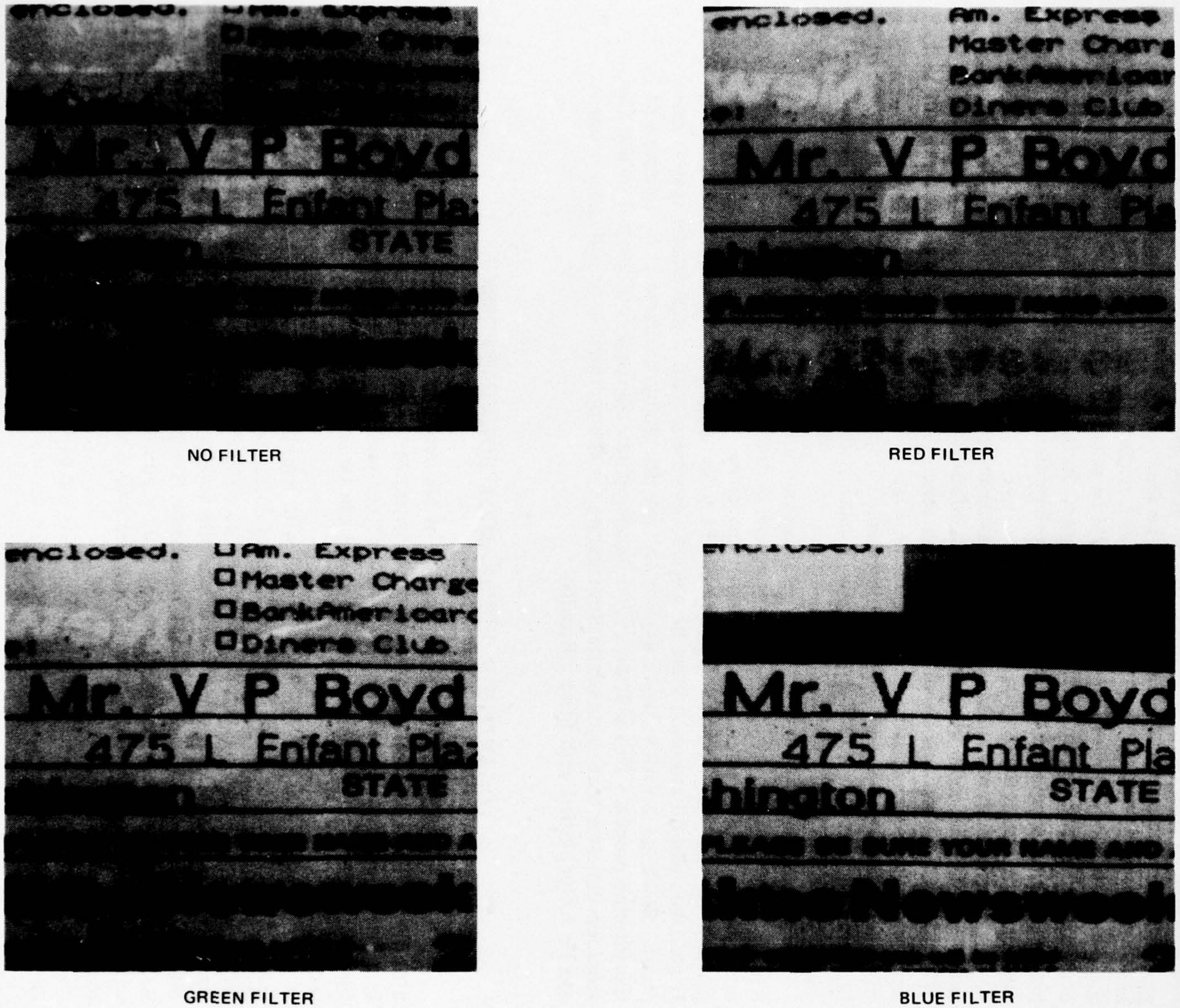


Figure E8. Effect of optical filtering on a multicolor document.

spaced voltages to the threshold devices. The alternative is to utilize the linearly spaced digital output steps of the A/D converter and to provide a "lookup table" in read only memory (ROM) form. The lookup table uses the A/D outputs as addresses for the ROM and the programmed data stored become the compressed output equivalent. The latter method has some drawbacks, since the fractional breakpoints for the ROM table are made at integer digitized values rather than at their true logarithmic fractional values. The method using the nonlinear A/D converter is being investigated under a Navy program at NELC, and the USPS will automatically obtain the benefits of the results. Therefore, values have been computed for the ROM table method and the results are discussed here. The Navy program will compress only from 6 bits to 5 log bits, so the USPS will evaluate the appearance of 6 bits compressed to 5 bits and also 4 bits.

To find the point of departure from the linear digitized values to the log steps, it is necessary to solve for the intercept point for the best fit of the straight line and the log curve. For the straight line portion, the value used is $n = B(n)$, (E1) where $B(n)$ is the brightness of the nth digitized value. In other words, the outputs of the A/D converter are used without modification. After the intercept point whose coordinates are n_o, B_o, logarithmic steps are taken in accordance with the equation

$$B_o (K + 1)^n = B(n). \tag{E2}$$

For a smooth transition between the two curves, the slopes must be equal at the point of connection. Therefore, the two first derivatives can be equated as follows:

$$\frac{d\,B(n)}{dn} = 1$$

$$\frac{dB(n)}{dn} = B_o (K + 1)^n \ln (K + 1) = B(n) \ln (K + 1) = 1$$

or

$$B(n) = \frac{1}{\ln(k + 1)} \tag{E3}$$

at the point B_o, as shown in the graph of figure E9.

$$B_o = 1/\ln (K + 1) = n_o \tag{E4}$$

and from equation (E2)

$$B_m = B_o (K + 1)^{(n_m - n_o)} = n_o (K + 1)^{(n_m - n_o)} \tag{E5}$$

$$\frac{B_m}{n_o} = (K + 1)^{(n_m - n_o)}$$

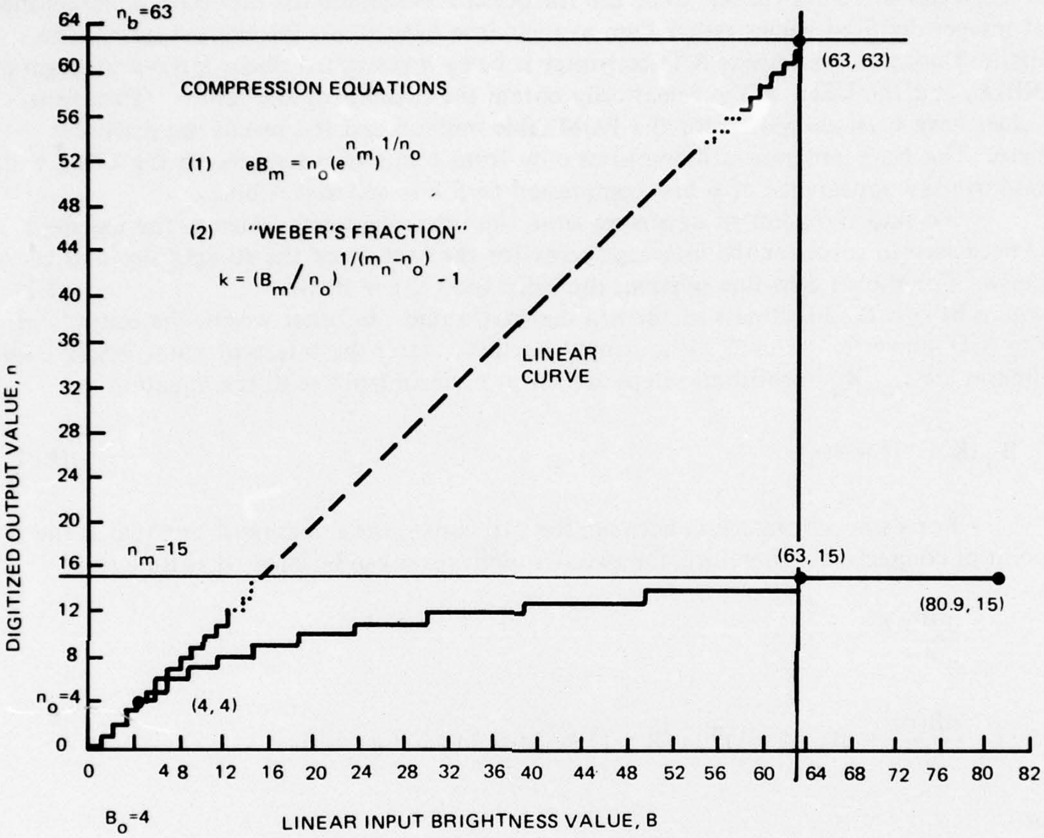


Figure E9. Video amplitude compression.

$$\frac{B_m}{n_o}^{1/(n_m - n_o)} = K + 1. \tag{E6}$$

Substituting (E6) into (E4) inverted,

$$\ln(K+1) = \frac{1}{n_m - n_o} \ln \frac{B_m}{n_o} = \frac{1}{B_o} = \frac{1}{n_o}$$

or

$$\ln\left(\frac{B_m}{n_o}\right) = \frac{n_m - n_o}{n_o} = \frac{n_m}{n_o} - 1$$

or

$$\frac{B_m}{n_o} - e^{\left(\frac{n_m}{n_o} - 1\right)} = e^{\frac{n_m}{n_o}} \cdot \frac{1}{e}$$

or

$$eB_m = n_o\, e^{n_m/n_o} = n_o p^{1/n_o} \text{ if } p = e^{n_m}. \tag{E7}$$

As an example, if 6-bit linear digital signals are log compressed to 4-bit digital signals, the value of $n_m = 16$ and the value of $B_m = 64$.

Solving equation (E7) for n_o,

$eB_m = 173.9700$ and $p + e^{n_m} = 8886110.5$

$173.97 = n_o\,(8886110.5)^{1/n_o}.$

Try $n_o = 4$.

$173.97 = 218.3926 + \epsilon.$

Try $n_o = 4.33$.

$173.97 = 174.2895 + \epsilon,$

which is close enough.

Solving for K + 1 by substituting in equation (E6) $\dfrac{B_m}{n_o}^{1/(n_m - n_o)} =$

$$\frac{64}{4.33}^{1/(16 - 4.33)} = K + 1 = 1.259594291.$$

Then the series becomes as follows (Table E1):

TABLE E1.

Six-digit Linear Value Breakpoint	Four-bit Binary Output	Remarks
0	0	
1	1	
2	2	
3	3	
4	4	
4.33		←end of linear
5.054	5	equivalence.
6.366	6	
8.017	7	$4.33 \times (K + 1)^{0.67} = 5.054$
10.100	8	
12.722	9	
16.025	10	
20.185	11	
25.425	12	
32.025	13	
40.338	14	
50.810	15	
63.999	16	

In this fashion a general table can be derived for 2-, 3-, 4-, and 5-bit breakpoints. Table E2 can be used for finding compressed values by entering the table at the left columns with the illumination corrected captured pel brightness value and reading the comparable compressed value from the appropriate adjacent column.

The table can be used for determining the companded equivalents of the original values. Companded values are those obtained by log compressing the digitized values for transmission and expanding back to linear values at the receiving site.

This is done by entering at the left columns as before and selecting an appropriate compressed value from one of the remaining columns. The companded values are then obtained by following the value downward to the arrow tip (if there is one) and utilizing the value in the far left column as the companded equivalent of the input number. In the absence of a vertical line and arrow beneath a selected compressed equivalent, the original value in the left column is also the companded value.

TABLE E2. STANDARD VIDEO COMPRESSION CONVERSION.

Illumination Corrected Captured PEL Brightness Values	Break Points for Companding: Two Bit	Three Bit	Four Bit	Five Bit
0.00	0	0	0	0
1		1	1	1
2		1	2	2
2.02		2		
2.33	1			
3			3	3
3.59		3		
4			4	4
5				5
5.05			5	
6				6
6.37			6	
6.39		4		
7				7
7.03	2			
8				8
8.02			7	
9				9
10				10
10.10			8	
11				11
11.37		5		
12				12
12.72			9	
13				
13.05				13
14				
14.19				14
15				
15.43				15
16				
16.02			10	
16.77				16
17				
18				
18.24				17
19				
19.38				18
20				
20.18			11	
20.23		6		
21				
21.21	3			
21.56				19
22				
23				
23.44				20
24				
25				
25.42			12	
25.49				21
26				
27				

24				
25				
25.42			12	
25.49				21
26				
27				
27.71				22
28				
29				
30				
30.13				23
31				
32				
32.02			13	
32.76				24
33				
34				
35				
35.62				25
35.98		7		
36				
37				
38				
38.73				26
39				
40				
40.34			14	
41				
42				
42.11				27
43				
44				
45				
45.79				28
46				
47				
48				
49				
49.79				29
50				
50.81			15	
51				
52				
53				
54				
54.14				30
55				
56				
57				
58				
58.86				31
59				
60				
61				
62				
63				
64	4	8	16	32

The granularity of the companded data is of course greater than that of the original data set, but the apportionment of the step sizes is made to minimize the cosmetic detractions to the observer.

A test was made using the frame store memory controller and a series of temporary lookup tables in the frame store memory. This test provides a capability to compare portions of an image which have been modified by the companding simulation algorithms on a side-by-side basis. Figure E10 is a photograph of the monitor showing the continuous tone girl portion of the IEEE facsimile chart. The actual image was captured in the prescan mode. The corresponding pel brightness data statistics show that all the captured image data lie between brightness levels 04 and 51. The pel brightness data table for the USPS facility photograph was also examined. The pel brightness data for this photograph were found to range between 09 and 40. The IEEE facsimile chart also contains fully saturated photographic blacks and whites for the line image portions of the chart. It was therefore assumed that the girl portion of the chart might be accommodated by brightness levels between 09 and 49.

A conversion table (table E3) was made to cover the range of the brightness values of the two images captured in the prescan mode. The extreme left column ranges through the 09 to 49 brightness levels. The next column contains the values biased in such a manner that 09 brightness as captured and corrected represents 00 for processing. The third column from the left contains the product of the second column and a gain constant, 1.561, which expands the video data to encompass the entire 64-bit dynamic range.

The processes accomplished in these left-hand columns will eventually be replaced by a combination of analog and digital circuits which have been designed to operate in real time.

The two pairs of columns remaining in table E3 contain the compressed video breakpoints and their companded equivalents. The center two columns contain data for compression from 6 bits to 4 bits. The right-hand two columns are to be used for 6-bit to 5-bit compression.

The girl image in figure E10 was made in part from data found in table E3. The top and bottom portions of the figure are generated directly from the illumination corrected prescan acquisition. In the next segment of the image, the 4-bit companded data from table E3 were used in the software program of the frame store memory controller. In this segment there are only 16 brightness levels from black to white. At least nine of these shades can be seen leftward from the highlight on the girl's forehead. The "contouring" of these brightness levels is quite noticeable.

Immediately below the 4-bit companded image the 5-bit companded data are presented. This section of course contains 32 brightness levels from black to white. A number of the levels are separately discernible with careful scrutiny, but the segment is much more pleasing to view becaue the contouring is hardly noticeable. The values of brightness used for this portion of the image were taken from the right-hand column of table E3.

The next segment below the 5-bit strip contains full 6-bit linear data. This portion of the image differs from the top and bottom strips because it has been linearly expanded to conform to the data in column three of table E3. There is very little difference between the 5-bit companded portion and the 6-bit linear strip. Some small changes can be seen across the bridge of the nose and the right cheek.

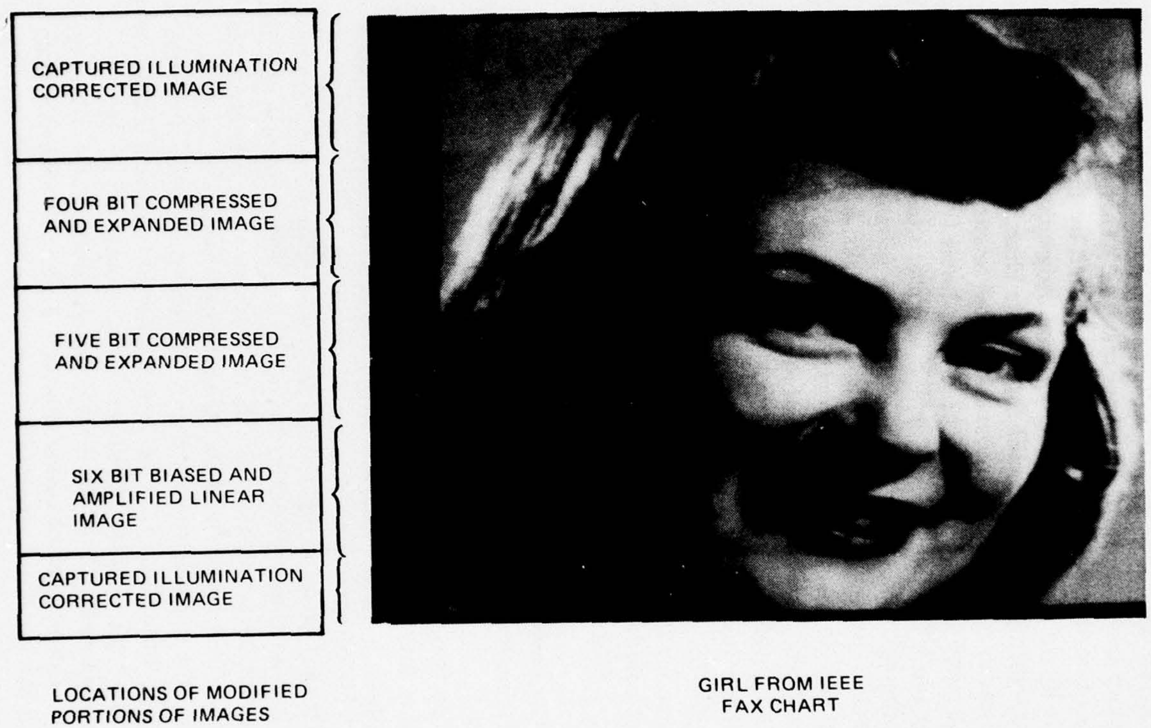


Figure E10. Effects of video companding on photographic image.

TABLE E3.
BIASED VIDEO COMPRESSION CONVERSION.

Illumination Corrected Captured Pel Brightness Values	Rebiased Pel Brightness Value	Expanded Pel Brightness Values	Four-Bit Equivalents	Companded Four-Bit Equivalents	Five-Bit Equivalents	Companded Five-Bit Equivalents
9	0	0.00	0	0.00	0	0.00
10	1	1.56	1	1.86	1	1.63
11	2	3.12	2	3.72	2	3.26
12	3	4.68	3	5.58	3	4.89
13	4	6.24	4	7.44	4	6.52
14	5	7.80	5	9.30	5	8.15
15	6	9.37	← 6	←11.27	6	9.78
16	7	10.93	← 7	←13.65	7	11.41
17	8	12.49	← 8	←16.52	8	13.04
18	9	14.05			9	14.67
19	10	15.61	← 9	←20.22	10	16.30
20	11	17.17			11	17.93
21	12	18.73			12	19.56
22	13	20.29	←10	←24.22	13	21.18
23	14	21.85			14	22.81
24	15	23.41	←11	←29.32	15	24.44
25	16	24.98			16	26.07
26	17	26.54			17	27.70
27	18	28.10			←18	←29.38
28	19	29.66	←12	←35.49	←19	←31.16
29	20	31.22			←20	←33.03
30	21	32.78			←21	←35.04
31	22	34.34			←22	←37.15
32	23	35.90	←13	←42.98		
33	24	37.46			←23	←39.39
34	25	39.02			←24	←41.78
35	26	40.59				
36	27	42.15	←14	←52.04	←25	←44.31
37	28	43.71			←26	←46.98
38	29	45.27				
39	30	46.83			←27	←49.82
40	31	48.39				
41	32	49.95			←28	←52.83
42	33	51.51	←15	←63.00		
43	34	53.07				
44	35	54.63			←29	←56.02
45	36	56.20			←30	←59.41
46	37	57.76				
47	38	59.32			←31	←63.00
48	39	60.88				
49	40	62.44				
50	41	64.00				

The amount of compression (if any) which should be used in a USPS imaging system will depend on a number of factors. It is obvious that amplitude compression can only eliminate 20–30% of video amplitude data. However, the video compression may in turn favorably affect the compressibility of the data when further compressed by run length encoding.

The dynamic range of most printing and display techniques is generally limited to 100:1 or less. Therefore, the acquisition of images using a 6-bit A/D converter and amplitude compressing to 5 or 4 bits appears to be a practical approach to amplitude resolution.

RESULTS AND CONCLUSIONS

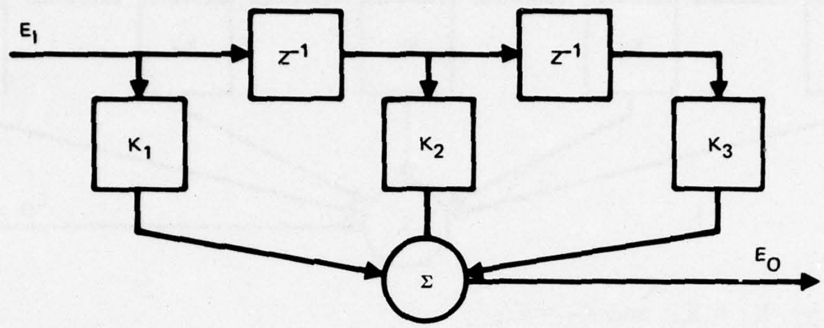
1. Two edge enhancement algorithms have been adapted to run on the image test bed.
2. The nonrecursive method of edge enhancement provides symmetry which the recursive filter does not.
3. A constant of K = 0.5 substituted in the nonrecursive algorithm suitably enhanced the test pattern and the soft focus sample of typed text.
4. The spectrum of the test bed illumination equipment appears to be adequate in spectral response for color filtering and color separation.
5. The proper choice of color filtering can greatly enhance paper to ink contrast ratio provided that the original copy is not just black and white.
6. Derivation of the equation for log compression using commercial A/D converters is presented.
7. Results of the compression and expansion calculations are tabulated in the report for future reference.
8. Portions of an image companded from 4 and 5 bits are compared on a side-by-side basis with unbiased, unexpanded prescan swatches and a strip of biased, expanded linear 6-bit image.
9. There is little difference between the 6-bit linear and the 5-bit companded portions of the image.
10. The image made from the 4-bit companded data contains noticeable contouring of the boundaries between brightness levels.

FUTURE NELC PLANS

1. Begin the design of the real-time edge enhancement circuits on a low-priority basis.
2. Continue to search the literature for other applicable enhancement techniques.
3. Now that the spectral bandwidth of the illumination has been verified, initiate a plan to provide a more efficient optical path for the imaging light. Consideration should be given to both increased intensity and uniformity of intensity across the data path.
4. For the 4-bit and 5-bit log compression equations, examine the possibility of combining the compression process with the illumination correction procedure so that both are done simultaneously and in real time.

APPENDIX A (TO TR 2020 APPENDIX E): NONRECURSIVE FILTER CALCULATIONS

For a two-pole filter, the configuration is:



$$E_o = E_I K_1 + E_I K_2 Z^{-1} + E_I K_3 Z^{-2}$$

$$\frac{E_o}{E_I} = \frac{K_1 Z^2 + K_2 Z + K_3}{Z^2} \qquad \text{(A1)}$$

For high-frequency enhancement (edge enhancement):

Desire a gain of +1 at low spatial frequencies (DC).

Desire a gain of perhaps –2 at the Nyquist limit

Then: $\frac{E_o}{E_I} = +1 \text{ @ } Z = +1$ and $\frac{E_o}{E_1} = -2 \text{ @ } Z = -1$

and for symmetry of response, $K_1 = K_3$.

Substituting into equation (A1) above:

$$K_1 + K_2 + K_3 = +1$$

$$K_1 - K_2 + K_3 = -2$$

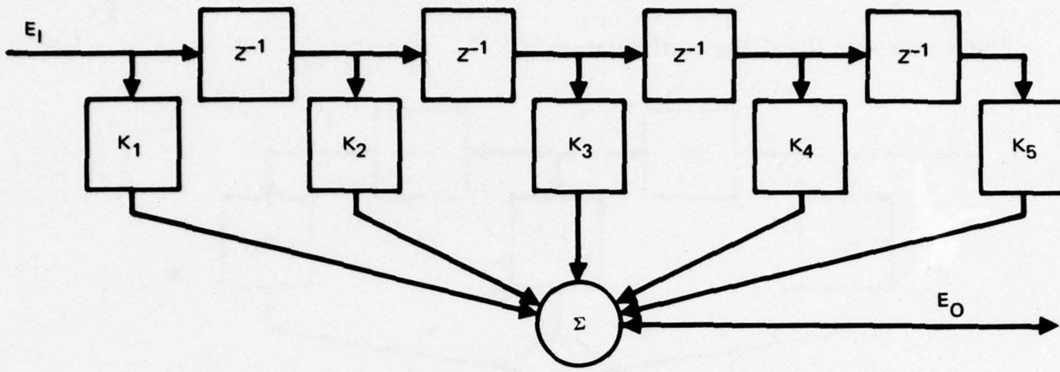
$$2K_1 + 2K_1 = -1 \qquad K_1 = -0.25 \qquad K_2 = +1.5$$

The gain at half Nyquist frequency where $Z = \pm j$ is

$$\frac{E_o}{E_I} = \frac{-K_1 \pm jK_2 + K_3}{-1} = \pm\, jK_2 \pm F\, j1.5.$$

The above performance calculations can be verified by graphical examples which follow. The zeros in the above equation lie at Z = +0.382 and Z = 2.618.

An investigation was also made for a four-pole nonrecursive filter as follows:



For symmetry, $K_1 = K_5$, and $K_2 = K_4$.

Since stroke widths of typed characters are about 2+ pels in width, the highest gain for edge enhancement should occur at $W_s/4$. At the Nyquist limit and at low spatial frequencies (DC), the gain should be +1. Therefore, for the equation

$$\frac{E_o}{E_I} = \frac{K_1 Z^4 + K_2 Z^3 + K_3 Z^2 + K_2 Z + K_1}{Z^4} \qquad \text{(A2)}$$

$$\frac{E_o}{E_I} = +1 @ Z = +1; \frac{E_o}{E_I} = +1 @ Z = -1; \frac{E_o}{E_I} = -2 @ Z = \pm j$$

Then:

$$2K_1 + 2K_2 + K_3 = +1$$

$$2K_1 - 2K_2 + K_3 = +1$$

$$2K_1 - K_3 = -2 \qquad \text{or} \qquad K_3 = 2K_1 + 2$$

$$K_1 = -0.25 = K_5$$

$$K_2 = 0.0 = K_4$$

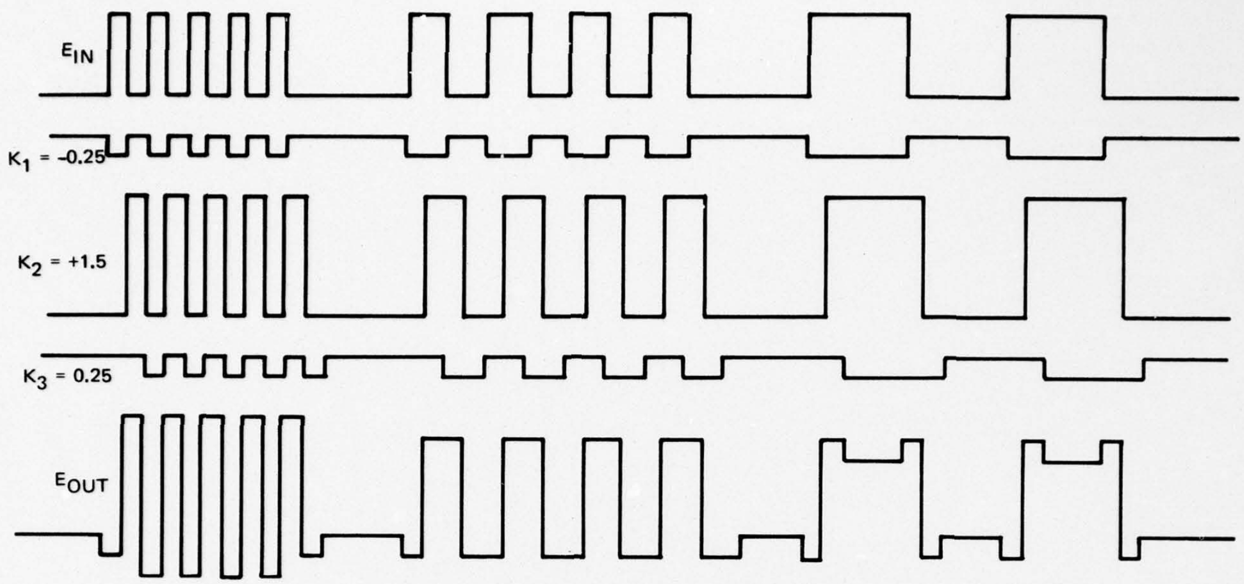
$$K_3 = +1.5$$

Hence, the desired equation is:

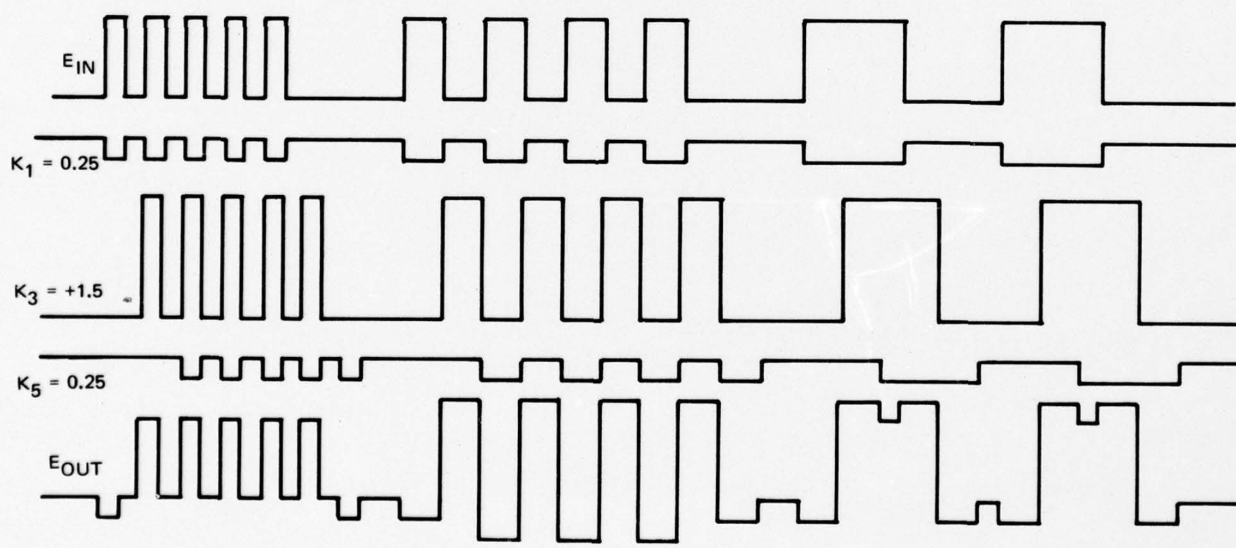
$$\frac{E_o}{E_I} = \frac{-0.25 Z^4 + 1.5 Z^2 - 0.25}{Z^4} .$$

The roots of the equation lie at Z = +0.41449 and Z = 2.41421. Wave forms of the response of this filter are given in comparison to the two-pole filter.

Response of the filter of equation (A1), given the selected values of K_1, K_2, and K_3, is as follows:



Response of the filter of equation (A2), given the selected values of K_1, K_2, K_3, K_4, and K_5, is as follows:



APPENDIX F: RELIABILITY PREDICTION REPORT
on the
SCANNING IMAGER ELECTRONICS

Prepared

for

US POSTAL SERVICE

September 1976

by
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INTRODUCTION

This report discusses reliability prediction criteria (as they apply to the scanning imager electronics being developed for the US Postal Service). The implications of variations of some of the more important parameters are also discussed. Computations are included based on the reliability formula presented, for small, medium, and large scale integration devices such as CCD scanners, ROMs RAMs, PROMs, and microprocessors.

Where available, manufacturer's device reliability data are presented for comparison to the theoretical calculations. It should be noted that manufacturers are, in general, treating scanning imagers like other medium to large scale integration devices as far as reliability is concerned. However, the Rome Air Development Center has funded a "Degradation Analysis of CCD/CID Devices" in their continuing efforts to keep MIL-HDBK-217B current.

This handbook is one of a series of military standardization handbooks. Its title is "Reliability Prediction of Electronic Equipment," dated 20 September 1974, and it is the basis for much of the theoretical discussion in this report. Although very conservative, the Handbook is widely used in industry and is the only approved guide for making reliability predictions for military equipment.

RELEVANCE TO DoD MISSION

Previous reports have reviewed the similarities between USPS imaging goals and the objectives of DoD. It follows that the military would be much concerned with the potential reliability of hardware using solid-state imaging devices. This report has in fact used the approved DoD reference, MIL-HDBK-217B, for making the MTBF predictions. Therefore, it is only necessary to adjust the final calculations for the environment of military usage of such equipment to have a report on the MTBF of scanning imager electronics for DoD missions.

RELIABILITY PREDICTION CONCEPTS

The design, fabrication, and development of large complex electronics equipment that is pushing and using the latest in the state of the art can well be considered to be revolutionary in nature as compared to the building of a simple amplifier for listening to records. Establishing a reliability figure of system failures per million hours is going to be much easier and far more accurate for the simple amplifier simply because every component has an established track record. The reliability predictions of failures per million hours could be taken as a statement of fact with a very high confidence level, whereas the reliability predictions for the very complex electronic systems must be considered for what they are – predictions. They most likely are based on extrapolations of data generated for generically similar devices.

The scanning imager electronics equipment certainly represents the state of the art in its incorporation and utilization of the latest in imagers, memory devices, and processors. The DoD Standardization Handbook, "Reliability Prediction of Electronic Equipment," MIL-HDBK-217B, dated 20 September 1974, from which much of the

following theoretical data were obtained, contains extensive data on micro-electronic devices, including bipolar and MOS devices and digital and linear devices, and covers complexities ranging from discrete logic elements to large scale integration devices. However, in spite of the volume of data the handbook contains, including formulae for making reliability predictions on equipment as large as desired, it must be kept in mind that the scanning imager electronics package may well contain one of the largest active memory banks ever conceived (25×10^6 bits), thus lowering the confidence level of any reliability predictions computed. Certainly the Handbook formulae were not developed by building and evaluating equipment of this complexity.

The Handbook describes two methods of predicting reliability: parts stress analysis and parts count. "Parts count" is the simpler approach that is frequently used in making proposals. It will not be discussed further in this report. "Parts stress analysis" is the method used and discussed in detail in this report. In addition to the limitation on type of failure analysis discussed, this report will only deal with the various integrated circuit semiconductor devices that may be encountered in the scanning imager electronics. Failure rate models and data are available for all types of devices required to build an operating electronics package and certainly must be considered in a complete failure analysis of an electronics system; however, that is beyond the scope of this report.

FAILURE RATE PREDICTION MODELS

The general failure rate prediction model for microelectronic devices, as given in MIL-HDBK-217B, is

$$\lambda_P = \pi_L \pi_Q (C_1 \pi_T + C_2 \pi_E) \qquad \text{(F1)}$$

where

λ_P is the part failure rate in failures per 10^6 hours,

π_L is the device learning factor, ranging from 1 for devices in full production to 10 for new devices in the development stages,

π_Q is the quality factor, ranging from 1 for the most stringent military specification grades to 150 for commercial grades,

π_T is the temperature acceleration factor, ranging from less than 0.1 to over 1000,

π_E is the application environment factor, ranging from 0.2 for very docile ground conditions to 10 for missile launch conditions, and

C_1, C_2 are the complexity factors, ranging from about 0.001 to about 10.

This model applies to bipolar and MOS, digital and linear, SSI to LSI (small scale integration to large scale integration), and memories. Tables and/or formulae are presented in appendix A (and MIL-HDBK-217B) to determine the values of each parameter for any type and size of microelectronic device. The π_L, π_Q, and π_E factors are fabrication or application oriented, whereas the C_1 and C_2 factors are tailored to specific device types and sizes. The π_T factor is both application and device oriented.

Equation (F1) gives a failure rate for one device such as a MOS random access memory or TTL shift register in terms of failures per million hours (the actual calculated value for λ_P could be much less than 1.0). It is not difficult to determine from the equation and the ranges for the various parameters that failure rates of tens to hundreds or even thousands per million hours could be generated for large developmental or commercial devices operated in adverse environment conditions. Conversely, relatively low failure rates can be obtained for production items made to rigid military specifications and operated in favorable environments, even for relatively large microelectronic devices.

To determine the expected MTBF (mean time between failures) for a piece of hardware, the general approach is to sum the failure rates for all the parts used in the piece of hardware and divide that sum into 1 million. Stated algebraically

$$MTBF = \frac{1\,000\,000}{N_{P_1}\lambda_{P_1} + N_{P_2}\lambda_{P_2} + N_{P_3}\lambda_{P_3} \ldots} , \qquad \text{(F2)}$$

where

MTBF is the mean time between failures in hours,

N is the number of parts of type P_1, P_2, or P_3, etc and

λ is the failure rate for parts of type P_1, P_2, or P_3, etc.

It can be deducted from equation (F2) that the MTBF of a piece of hardware will become less as the number of parts goes up. However, from the discussions so far, it is not apparent that it may be desirable to use larger microelectronic devices in order to cut down the number of individual devices. This comes about in the methods used for determining the complexity factors. SSI, MSI, linear, and memories all use the form

$$C = K_O N^{K_1} , \qquad \text{(F3)}$$

where

C is the complexity factor,

K_O is a constant,

K_1 is a constant ranging from 0.35 to 0.76, and

N is the number of transistors, gates, or bits as appropriate.

The value of K_1 being less than 1.0 is the key. For any failure rate prediction model that calculates the complexity factors in a manner equivalent to equation (F3), it is desirable to use as large a micro-electronic device as can be obtained.

For LSI devices the method of calculating the complexity factors is of the form

$$C = K_O e^{K_1 G} , \qquad \text{(F4)}$$

where

e	is the base of natural logarithms, 2.718,
K_O, K_I	are constants, and
G	is the number of gates in the device.

With this form of complexity factor calculation, the increase in the value of C is slower than the increase in number of gates only up to about 250 gates (LSI is considered 100 gates or larger) using the presently accepted value for K_1. In the range of 250 to about 1350 gates the value of C still does not get too large; but above 1400 gates, in a LSI device, the value of C begins to grow at a rate that suggests such devices are not practical. (The Handbook appears to be excessively conservative for large LSI devices.)

The complexity factors have been discussed at length because they are the ones of most interest in determining hardware implementation philosophy for very large and sophisticated systems such as the scanning imager electronics. Careful analysis of different hardware implementation concepts could make a significant difference in MTBF figures based solely on how different microelectronic devices affect the complexity factors.

The π_L, π_Q, π_E, and π_T factors have just as much effect on MTBF as the complexity factors, but there is very little subtlety in their application. It is obvious that it is best to choose a device that has been in production for some time and is made to rigid standards for low π_L and π_Q values, respectively. The environment factor, π_E, is not usually subject to change. If a system has to work while airborne, that is where it has to work and the π_E factor is thus determined. The temperature acceleration factor, π_T, is somewhat more subtle. Obviously, the temperature of the operating environment can be controlled in most applications by some means. The subtlety of this factor comes about in that the types and sizes of microelectronic devices chosen for the hardware implementation can be significant in determining the actual microelectronic device junction temperature upon which π_T is based.

RELIABILITY PREDICTION COMPUTATIONS

In this section failure rates will be calculated for various microelectronic devices typical of those used in the scanning imager electronics and then these failure rates will be used to arrive at a MTBF figure for the entire scanning image electronics package. Where practical, various combinations of devices will be considered; ie, a memory bank using many small devices versus a few large devices doing the same task. It should be kept in mind that the reliability prediction models being used will, of necessity, be conservative, thus producing low MTBF figures. It would serve no useful purpose to generate overly optimistic figures. It would be reasonable to assume that the figures arrived at will be worst case.

In the computations that follow, the π_L, π_Q, and π_E factors will always be the same, so a set of values will be assigned to them now and entered into equation (F1). The values are 1.0, 5, and 1.0, respectively. Thus equation (F1) becomes

$$\lambda_p = (1.0)(5)[C_1 \pi_T + (C_2)(1.0)]$$

$$= 5(C_1 \pi_T + C_2). \qquad \text{(F5)}$$

The reasoning used in determining the above factors is discussed in the following five paragraphs.

It was stated earlier that the learning factor, π_L, had a range of 1 to 10. (The handbook actually says the value of π_L is either 1 or 10.) A value of 1 will be used because it can be assumed that by the time any hardware goes into production the learning process is over. Any devices selected for use in the scanning imager electronics should definitely be production items.

The value chosen for the quality factor, π_Q, is a little more difficult to determine. It would be easy to just say, "use the best parts possible," but that is not reasonable. The choice of parts quality assurance level, ie π_Q, has a significant effect on the cost of the parts. The range was given as 1 to 150. The 150 is for commercial grades, which are definitely unacceptable. For high-quality parts, the handbook shows five categories based on testing, fabrication, and manufacturing controls for which the π_Q factor ranges from 1 to 16.

The lowest "class" of quality parts, class C, which receives the π_Q value of 16, does not receive any burn-in screening. The next better class is B2, for which π_Q is 10. This class of parts receives a burn-in screening and such other tests called out in MIL-STD-883, Method 5004, Class B, as the vendor considers important. Class B1 parts, which receive a π_Q of 5, have received all the testing called out in MIL-STD-883, Method 5004, Class B, including the same burn-in screening that Class B2 parts receive. The full Class B parts, for which π_Q is 2, have certain restrictions put on the manufacturing and fabrication processes in addition to passing tests required of class B2 parts. Class A parts, the very best that industry can produce, receive a π_Q value of 1. These parts receive a longer burn-in and have even more stringent restrictions on manufacturing and fabrication. Vendors supplying class A and B parts must be certified as being qualified and must be recertified periodically to keep their status.

The value for π_Q was set at 5, the value given to class B1 parts. The reasoning is that these parts have received the full MIL-STD-883 testing, which includes a significant burn-in. It probably is premature to consider that the fabrication restraints of full class B parts could be applied to the very large memory devices. Certainly full class B parts are going to be considerably more expensive – on the order of 5 times. Class B2 parts with a π_Q of 10 would also be a good choice if costs become a significant factor. (Hughes Aircraft has extensive data to show that their delivered hardware will have MTBF figures commensurate with full class B parts even though they have used class C parts and in some instances class D parts. This is attributed to the fact that the operating time accumulated by the time the equipment is delivered is sufficient to produce the effect of class B screening.)

The range of the environment factor, π_E, was given as 0.2 to 10. Table 2.1.5-3 in appendix A lists several categories and associated values for π_E. The category that is most appropriate for this application is "ground, fixed" with a value of 1.0 for π_E.

The π_T factor is a computed factor that is dependent on three items: ambient temperature, device size, and device type. The ambient temperature will be, in the end, determined by the equipment design and/or the operating environment. For the purposes of this report it will be assumed that the ambient will be controlled to 50°C. The device size affects the computations in that the size generally affects the level above ambient at which the device junctions operate. This information is generally available for microelectronic devices; however, the Handbook gives a guideline in the absence of actual data, ie, 10°C for devices with no more than 120 transistors and 25°C for devices with more than 120 transistors. For this report the junction

temperature, T_j, used for all computations will be either 60°C or 75°C. The device type determines which of two T_j values are used in the π_T computations.

The expression for π_T is

$$\pi_T = 0.1\ e^X\ , \tag{F6}$$

where

e is the natural log base, 2.718, and

$$X = (-)\,(K_1 \text{ or } K_2)\ \frac{1}{T_j + 273} - \frac{1}{298}\ . \tag{F7}$$

T_j is the junction temperature in °C (60° or 75° for this report);

K_1 = 8121 for bipolar and MOS linear, bipolar beam lead, bipolar ECL, and all other MOS devices; and

K_2 = 4794 for bipolar digital devices, ie, TTL, DTL, and devices not included by K_1.

Using the values stated above for T_j, the values for π_T are calculated and presented in table F1. Unless specifically noted, all the computations in the rest of this report will use one of the tabulated values.

TABLE F1.

Devices Types	π_T T_j = 60°C ≤ 120 transistors	π_T T_j = 75°C > 120 transistors
K_1 BP and Mos linear, BP beam lead, BP ECL, and all other MOS	1.75	5.04
K_2 BP digital (ie, TTL, DTL, and devices not included in K_1)	0.54	1.00

SCANNING IMAGER ELECTRONICS

The scanning imager electronics, for which the following computations are made, is a hypothetical electronics package modeled after the hardware built by NELC Display Division. The NELC hardware is capable of storing (in active memory) only about one-eighth of a page at a time of 6-level Gray scale data. The system envisioned for the computations of this report will be capable of full-page storage. The complement of microelectronic devices required for this system is given in table F2. In the following

sections λ_p, failure rate per million hours, will be calculated for each of the 10 device types listed. Then an MTBF figure will be compiled for the entire package.

TABLE F2. SCANNING IMAGER ELECTRONICS MICROELECTRONICS COMPLEMENT.

		LSI		SSI/MSI		Memory/CCD	
Device	Technology	qty	Equiv no Gates	qty	Equiv no Gates	qty	bits
Main processor							
CCD imager	MOS					1	1700
INTEL 3001	TTL	1	250				
INTEL 3002	TTL	24	250				
INTEL 3003	TTL			3	30		
MMI 6306	TTL					12	ROM 2048
Misc	TTL			100	50		
Misc	TTL			200	20		
Memory bank							
T1 TMS4030	MOS					6000	RAM 4000
Alternate device	MOS					1500	RAM 1600
Alternate device	MOS					375	RAM 64 000
Image analyzer	ECL					24	RAM 64
Misc	ECL			250	10		

LARGE SCALE INTEGRATION

MIL-HDBK-217B defines LSI as being a device that is equivalent to 100 gates or larger. One gate is assumed to use four transistors and a J-K or R-S flip-flop is considered to have 8 gates. By definition, memory devices would be considered LSI; however, the Handbook provides a separate reliability prediction model for them. Therefore, for the balance of this report, LSI will include only those large digital microelectronic devices that are not considered to be memory devices. Microprocessor and arithmetic devices would (as of this report date) be considered LSI. Charge coupled and charge injection imaging devices are also LSI devices by the above definition. The Handbook makes no mention of such devices; however, it is the judgment of this author that they should be considered ROM type memory devices for reliability prediction purposes. They are laid out in the orderly fashion of a memory device as opposed to the random configurations encountered in other LSI devices, and they are more like ROM in that they receive only signals for outputting.

Section 2.1.3 of appendix A provides the necessary information to apply equation (F5), which is repeated here, to the LSI devices in table F2.

$$\lambda_P = 5 \; (C_1 \pi_T + C) \qquad \text{(F5)}$$

$$C_1 = 0.0187 \; e^{0.005G} \qquad \text{(F8)}$$

$$C_2 = 0.013 \; e^{\;0.004G} \qquad \text{(F9)}$$

$$\pi_T = \text{See table 1}$$

In table F2 there are two LSI devices listed; however, both types have 250 gates, and they are both TTL technology, so only one λ_P calculation is necessary. From table F1 the π_T value is determined to be 1.00. Therefore, computing C_1 and C_2

$$C_1 = 0.0187 \; e^{(0.005)\,(250)}$$

$$= 0.0653$$

$$C_2 = 0.013 \; e^{(0.004)\,(250)}$$

Putting all of values determined into equation (F5)

$$\lambda_{LSI} = 5 \; [\,(0.0653)\,(1.00) + 0.0353]$$

$$= 0.503 \text{ failure per } 10^6 \text{ hours}$$

MEMORY DEVICES

From section 2.1.4, appendix A, the expressions for C_1 and C_2 for ROMs are

$$C_1 = 0.00114 \; B^{0.603} \qquad \text{(F10)}$$

$$C_2 = 0.00032 \; B^{0.646}, \qquad \text{(F11)}$$

and for RAMs

$$C_1 = 0.00199 \; B^{0.603} \qquad \text{(F12)}$$

$$C_2 = 0.00056 \; B^{0.644} \qquad \text{(F13)}$$

There is only one type of ROM listed in table F2 and it is TTL with 2048 bits. From table F1 the value of π_T is determined to be 1.00. C_1 and C_2 are computed to be 0.1131 and 0.04408, respectively. Putting these values into equation (F5)

$$\lambda_{ROM} = 5 \; [\,(0.1131)\,(1.00) + 0.0441]$$

$$= 0.786 \text{ failure per } 10^6 \text{ hours}$$

There are three sizes – 4000, 16 000, and 64 000 bits – of MOS RAM listed in table F2 and one size, 64 bits, of ECL RAM. From table F1, the π_T value is 5.04 for all devices. C_1 and C_2 for each of the four devices are computed to be:

	64 ECL	4k MOS	16k MOS	64k MOS
C_1	0.02443	0.29571	0.68221	1.5733
C_2	0.00815	0.11692	0.28551	0.6969

Using equation (F5), the λ_P values are computed to be

$$\lambda_{64\ RAM} = 0.6564 \text{ failure per } 10^6 \text{ hours,}$$

$$\lambda_{4k\ RAM} = 8.036,$$

$$\lambda_{16k\ RAM} = 18.619, \text{ and}$$

$$\lambda_{64k\ RAM} = 43.131.$$

CCD SCANNING IMAGER

It was stated earlier that the charge coupled device used for image scanning would be treated like a ROM for failure rate prediction purposes. Therefore, equations (F10) and (F11) are appropriate for C_1 and C_2 calculation and π_T is determined to be 5.04 from table F1. C_1 and C_2 are computed to be 0.1765 and 0.0391, respectively. The λ_P then computes to be

$$\lambda_{CCD} = 5\ [\ (0.1765)\ (5.04)\ + 0.0391]$$

$$= 4.64 \text{ failures per } 10^6 \text{ hours.}$$

MEDIUM/SMALL SCALE INTEGRATION

From section 2.1.1, appendix A, the expressions for C_1 and C_2 are

$$C_1 = 0.00129\ G^{0.67} \quad \text{and} \qquad \text{(F14)}$$

$$C_2 = 0.00389\ G^{0.35} \qquad \text{(F15)}$$

There are three sizes – 20, 30, and 50 equivalent gates – of MSI/SSI TTL devices listed in table F2 and one size of ECL device. From table F1, the π_T values are 0.54 for the 20- and 30-gate TTL devices, 1.00 for the 50-gate TTL device, and 1.75 for the ECL device. The computed values of C_1 and C_2 for the various devices are

	TTL 20	TTL 30	TTL 50	ECL 10
C_1	0.0096	0.0126	0.0177	0.0060
C_2	0.0111	0.0128	0.0153	0.0087

Using equation (F5), the computed values of C_1 and C_2, and the values for π_T, the λ_p values are computed to be

$$\lambda_{20}\ \text{TTL} = 0.0814 \text{ failure per } 10^6 \text{ hours},$$
$$\lambda_{30}\ \text{TTL} = 0.0980,$$
$$\lambda_{50}\ \text{TTL} = 0.1650, \text{ and}$$
$$\lambda_{10}\ \text{ECL} = 0.0960.$$

SCANNING IMAGER ELECTRONICS MTBF

The MTBF for the scanning imager electronics is computed using equation (F2), which is repeated below.

$$\text{MTBF} = \frac{1\ 000\ 000}{N_{P_1}\lambda_{P_1} + N_{P_3}\lambda_{P_3}} \text{ hours} \tag{F2}$$

The number of parts of each type of microelectronic device is determined from table F2, and the λ_p values have just been calculated for the various devices. In table F3 the total failures per million hours have been determined for each type of device. In table F4 an MTBF has been determined, according to equation (F2), for the scanning imager electronics for three different memory bank devices.

TABLE F3. SCANNING IMAGER ELECTRONICS FAILURES PER 10^6 HOURS.

Device	Np	λp	Npλp
CCD imager	1	4.64	4.64
Intel 3001	1	0.503	0.50
Intel 3002	24	0.503	12.07
Intel 3003	3	0.098	0.29
MM1 6306	12	0.786	9.43
Misc TTL	100	0.1650	16.50
Misc TTL	200	0.0814	16.28
TMS4030 4k RAM	6000	8.036	48216.0
Alternate 16k RAM	1500	18.619	27928.0
Alternate 64k RAM	375	43.131	16174.0
ECL RAM	24	0.6564	15.75
Misc ECL	250	0.0960	24.00

TABLE F4. SCANNING IMAGER ELECTRONICS MTBF.

Device	Memory Bank Failures	Failures Per 10^6 Hours All Other Parts	Sum of Failures	MTBF. hours
4k RAM	48216	99.46	48316	20.7
16k RAM	27928	99.46	28028	35.7
64k RAM*	16174	99.46	16274	61.4

*Acceptable 64k RAM may not be available in the required time frame.

The computed MTBF figures, 21 to 61 hours, for the hypothetical scanning imager electronics – even using futuristics 64 000-bit memory chips – is definitely undesirable and most likely unacceptable. Such low figures do not mean that there is no hope. Several facts should be kept in mind and examined for methods of improvement, including:

1. The numbers are predictions based on a conservative approach.
2. The best parts possible (π_Q = 5 was used) were not used in the computations.
3. The system MTBF is controlled entirely by the memory bank.
4. The temperature acceleration factor, π_T, is a significant factor in the computations.
5. Actual reliability figures for the various devices may be one to two orders of magnitude better (see the following section on manufacturer's data).

Taking the above statements in order, the first deals with the degree of conservatism built into MIL-HDBK-217B. There is the possibility that actual practice may produce a factor of 10 improvement, but that could only be determined after the fact, which could be an expensive gamble if the improvement did not materialize. The confidence level in such a venture is put at less than 10%. A 2:1 improvement is much more palatable – the confidence level on this is put at 90%, thus producing MTBF times of 41, 71, and 123 hours.

Class B1 parts were selected, giving a π_Q of 5. This factor is inversely proportional to MTBF, thus very effective. Reduce π_Q by a factor of 2 and MTBF goes up by 2. This looks good at first glance but at best can give only 5:1 improvement – Class A parts used in satellites only reduce π_Q to 1 and the cost is definitely unattractive. One of the most important factors in screening parts for a better quality assurance class is burn-in time. An alternative to buying better parts is to have the equipment manufacturer continue to burn-in the hardware before delivery for 200 or more hours after the last part failure. This procedure could produce an effective π_Q of at least 2.5 with a confidence level of 90%. This would put the predicted MTBFs at 82, 142, and 246 hours – still not at all attractive, particularly if the 64k RAM device is not available.

Comparison of columns one and two in table F4 shows the number of failures per million hours for the memory bank to be more than a hundred times greater than for all the other parts put together – 280 to 480 times for devices available today. With this in mind, it would do nothing to the confidence level of the predictions if the parts outside the memory bank had an infinite life prediction. It was in anticipation of this

condition that alternative failure rate predictions were made only for the memory bank devices. Choosing devices that were 4 and 16 times larger than the devices used in the NELC hardware resulted in MTBF figures that were 1.7 and 3.0 times better, respectively. Acceptable 16k devices are currently available; however, 64k devices are not. It would have required memory elements with a million bits for the initial MTBF prediction to have been about 200 hours. Such devices are definitely a long way off. What this boils down to is that making larger devices will solve the problem but is not a practical approach. What is needed is a type of memory device technology that is inherently better in reliability by a factor of 10 or more.

The temperature acceleration factor, π_T, appears to offer the best possibility for MTBF improvement. In the discussion of π_T, ambient temperature ie, the temperature at the mounting surface of the microelectronic devices was set at 50°C (122°F). This produced a π_T of 5.04 for large MOS devices. By lowering the ambient temperature 10°, π_T will be reduced by a factor of 2, and a 15° reduction would reduce π_T by a factor of 3. In the MTBF computations for the scanning imager electronics these reductions in π_T would produce a 200 or 300% increase in MTBF. Such reductions would definitely require special cooling techniques and would add significantly to the manufacturing cost. A 3:1 improvement in π_T produces MTBFs of 246, 426, and 738 hours for each of the three memory devices. These figures include the two previous factors discussed for MTBF improvement.

It was suggested in a previous paragraph that a device with inherently better reliability was needed to make a substantial improvement in the MTBF prediction. This comment was directed to the complexity factors, C_1 and C_2, when first made, but it could also be directed to the π_T factor. Referring back to the discussions on π_T and table F1, it can be seen that a 5:1 improvement in π_T of the memory devices and, consequently, the MTBF of the scanning imager electronics could be obtained if the K_2 constant were used instead of K_1. K_2 applies to bipolar digital devices including DTL, TTL, and, in the judgment of this author, I^2L (integrated injection logic). At the time the Handbook was written, I^2L was not generally available so was not mentioned in the definitions. The technology is, however, definitely based on bipolar semiconductor materials and will no doubt be included in the next revision of the Handbook. Actually, a memory device using DTL or TTL would, theoretically, give the same MTBF improvement; but these are not practical technologies for such LSI devices. Large I^2L memory devices are practical, however, and they will be able to meet the access time requirements. Another benefit to using I^2L technology over MOS is a probable reduction in power dissipation by about 2:1 in a dynamic mode; ie, while data are being processed and the memory is being refreshed (the TMS4030 devices require continuous refresh). This power reduction does not change the reliability predictions, but it makes it easier to maintain a given temperature, which does affect reliability. It should be noted that the memory for the scanning imager electronics, using the TMS4030 devices, would dissipate 3 to 5 kilowatts. In summary, the use of I^2L devices in the memory bank could

1. Improve the MTBF predictions to 410, 710, and 1230 hours for the three sizes of memory devices,
2. Reduce total power consumption, and
3. Reduce cooling requirements.

Unfortunately, 4k devices are just starting to come on the market, so the larger devices may not be available in the required time frame. The MTBF predictions for the hypothetical scanning imager electronics started out at a low of 20.7 hours and went up to 1230 hours. Table F5 summarizes the various values and the changes requied to get the improved MTBF figures.

TABLE F5. SCANNING IMAGER ELECTRONICS MTBF – IMPROVED VERSIONS.

	MTBF hours		
Method of Improvement	4k RAM	16k RAM	64k RAM
Calculations from table F4	20.7	35.7	61.4
Taking some conservatism out of the calculations – a factor of 2:1	41	71	123
Improved π_Q by a factor of 2:1	82	142	246
Reduce ambient temperature by 15°C to 35°C thus lowering π by a factor of 3:1	246	426	738
Use I^2L memory devices in-lieu of reducing ambient temperature	410	710	1230
Use I^2L memory devices and lower ambient temperature 5°C	492	852	1476
Use I^2L memory devices and lower ambient temperature 10°C	615	1065	1845

RECENT IMAGER DEVELOPMENTS

There are three principal manufacturers of off-the-shelf solid-state imagery devices – RCA, Reticon, and Fairchild. Their imagers most nearly compatible with USPS requirements are the SID51232, RL 1872F, and CCD 131CD, respectively.

RCA has made design improvements on the SID 51232 by replacing the surface channel horizontal output register with a buried-layer equivalent. This improves the performance of the device somewhat but does not contribute significantly to reliability improvement.

There have been persistent rumors throughout the CCD imager industry that plastic packages and seals can and do lead to degradation of performance of the devices. Fairchild has offered for sale new versions of the CCD 121CD (the 1728 pel device) and the CCD 131CD (the dual-ported 1024 pel device operating at 12 megapels per port) which are hermetically sealed in new dual in-line packages (DIPs). This type of package should greatly improve the useful life of devices from the standpoints of both chemical surface contamination/corrosion and possible humidity condensation on the inside of the quartz imaging window.

There exists a great deal of latitude in the value of MTBF which can be obtained for an imaging device. Using MIL-HDBK-217B, many values of MTBF can be calculated. If one assumes a high complexity factor C, and a high device learning factor π_L, the MTBF estimate may be as high as 100 failures per 10^6 hours. Lower factor choices may provide about 18 failures per 10^6 hours. Actual life tests by a manufacturer may yield estimates on the order of 0.5 failure per 10^6 hours.

WARRANTIES

Warranties on CCD devices are almost nonexistent. RCA offers a 90-day warranty on the CCD cameras and imagers. The Lancaster marketing manager for the product line explains that the items are covered under paragraph 7(a) of RCA Lancaster Terms and Conditions, IVM-2, dated 8-30-76. A copy of paragraph 7 is reproduced with permission in appendix B. RCA considers these products to be developmental items. Consequently, under the specific adjustment terms referenced in paragraph 7(a), the limited warranty period is set at 90 days. A copy of the limited warranty is also reproduced with permission in appendix B.

In the not too distant future when these items become commercial production units, the warranty will probably be extended to 1 year, provided that the claim is made within 18 months of the purchase. This latter clause allows the purchaser a 6-month acquisition holding period before the equipment is powered up.

Fairchild does not warrant their devices but publishes a data sheet with a Polaroid photo of a scope trace showing the performance of the imager at recommended clock voltages. A sample is shown in appendix C. The reaction of the company to a customer claim of premature failure of a device is not known at this time. Presumably Fairchild would analyze the device under a microscope to try to determine whether the failure was due to abuse or workmanship. Other campanies might also follow the same approach.

CONCLUSIONS

1. The MTBF of the scanning imager electronics model used is 82 hours.
2. The principal contributor to the MTBF duration is the failure rate of the random access memory (RAM) devices.
3. This dependency on the RAM device failure rate is due to the large number (6000) required).
4. The MTBF of the same equipment can be increased to 246 hours by using 64k RAM devices.
5. The MTBF of the same equipment can be further increased to 1230 hours by using integrated injection logic (I^2L) memory devices.
6. The reliability of the imaging devices does not measurably alter the MTBF of the model equipment.
7. The MIL-HDBK-217 reliability predictions for semiconductor components are extremely conservative. The NELC test bed memory is about one-eighth the size of a full memory used in the model equipment. There has been one memory failure in 1475 hours of operation, whereas the calculated value using MIL-HDBK 217B would have been about nine failures in this same time period.

MIL-HDBK-217B
20 SEPTEMBER 1974
SUPERSEDING
MIL-HDBK-217A
1 DECEMBER 1965

MILITARY STANDARDIZATION HANDBOOK

RELIABILITY PREDICTION OF ELECTRONIC EQUIPMENT

FSC-MISC

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1.0 INTRODUCTION

1.1 The Reliability Problem

When it is proposed to design an electronic system to perform a complex and demanding job, it is assumed that the required investment will be justified according to the perfection by which the job is performed or by the large number of times which the system can do the job. This assumption cannot be justified when a system fails to perform upon demand or fails to perform repeatedly. Thus, it is not enough simply to show that a chasm can be spanned by a bridge; the bridge must continue to span the chasm for a long time to come while carrying useful loads.

In the design of complex electronic systems, such an assumption as mentioned above, is, in fact, not accepted. Instead, considerable effort is made to obtain reliable system performance. Unlike bridge building and other evolving technologies, it is recognized that the electronics art, especially complex military systems, is often in revolution. It is sometimes referred to as an exploding technology. Without time for orderly evolution of systems, applications of electronics suffer most from unreliability. The ratio of new to tried and true portions of electronic systems is relatively high; therefore, until the new becomes tried and true, its reliability must be suspect. As an inevitable but not suprising result, it can be concluded that reliability remains a special problem in electronics and will remain so, as long as the technology is in revolution rather than evolution.

Reliability is a problem at all levels of electronics, from materials to operating systems, because materials go to make up parts, parts compose assemblies, and assemblies are combined in systems of ever increasing complexity and sophistication. Therefore, at any level of development and design, it is natural to find the influence of reliability engineering acting as a discipline founded to devote special engineering attention to the unreliability problem. Reliability engineering is concerned with the time degradation of materials, physical and electronic measurements, equipment design, processes and system analysis, and synthesis. None of these can be isolated from the overall electronics context, but must be carried on in conjunction with many other disciplines.

1.2 The Role of Reliability Prediction in Engineering

To be of value, a prediction must be timely. However, the earlier it is needed the more difficulties will be encountered. It is certainly true that the earlier a prediction has to be made about the unknown nature of a future event the more difficult it is to make a meaningful prediction. As an example, it can be seen that the reliability of an electronic equipment is known with certainty after it has been used in the field until it is worn out and its failure history has been faithfully recorded. But for purposes of doing anything about the reliability of this equipment, this knowledge has no value. Before this point, reliability cannot be known with certainty; but a great deal of knowledge about reliability can be accumulated over a short early period in the equipments' useful life. Eventhough the degree of certainty of knowledge is less, there is some opportunity to do something to influence the reliability of the remaining life portion.

The use of failure rate data, obtained from field use of past systems, is applicable on future concepts depending on the degree of similarity existing both in the hardware design and in the anticipated environments. Data obtained on a system used in one environment may not be applicable to use in a different environment, especially if the new environment substantially exceeds the design capabilities. Other variants that can affect the stated failure rate of a given system are: different uses, different operators, different maintenance practices, different measurement techniques or definitions of failure. When considering the comparison between similar but unlike systems, the possible variations are obviously even greater.

Thus a fundamental limitation on reliability prediction is the ability to accumulate data of known validity for the new application. Another fundamental limitation is the complexity of prediction techniques. Very simple techniques omit a great deal of distinguishing detail and the prediction suffers inaccuracy. More detailed techniques can become so bogged down in detail that the prediction becomes costly and may actually lag the principle hardware development effort.

This revision of the Handbook includes two methods of reliability prediction - "Part Stress Analysis" in Section 2 and "Parts Count" in Section 3. These methods vary in degree of information needed to apply them. The Part Stress Analysis requires the greatest amount of detail and is applicable during the later design phase where actual hardware and circuits are being designed. The Parts Count Method requires less information, generally that dealing with quantity of different part types, quality level of the parts, and the application environment. This method is applicable in the early design phase and during bid proposal formulation. Both methods will be revised periodically and new prediction methods will be added as they are developed. The Appendices contain guidelines for system and equipment reliability modeling and useful approximations for reliability calculations.

The failure rates presented herein represent the best available knowledge at the time of issue. Reliability predictions performed for military agencies should use no other source of data unless specifically approved by the procuring activity.

2.0 PART STRESS ANALYSIS PREDICTION

a. Applicability.

This method is applicable when most of the design is completed and a detailed parts list including part stresses is available. It can also be used during later design phases for reliability tradeoffs vs. part selection and stresses. This section contains failure rate models for a broad variety of parts used in electronic equipment. The parts are grouped by major categories and, where appropriate, are sub-grouped within categories. The major categories are listed in Table 2-1.

Table 2-1 MAJOR PART CATEGORIES FOR PART STRESS ANALYSIS

PART CATEGORY	SECTION
Microelectronics	2.1
Discrete Semiconductors	2.2
Tubes	2.3
Lasers	2.4
Resistors	2.5
Capacitors	2.6
Inductive	2.7
Rotary	2.8
Relays	2.9
Switches	2.10
Connectors	2.11
Wire & Printed Wire Boards	2.12
Miscellaneous (includes connections)	2.13

b. Part Quality.

The quality of a part has a direct effect on the part failure rate and appears in the part models as a factor, π_Q. Many parts are covered by specifications that have several quality levels, hence the part models have values of π_Q that are keyed to these quality levels. Such parts with their quality designators are shown in Table 2-2. The detailed requirements for these levels are clearly defined in the applicable specification.

TABLE 2-2 PARTS WITH MULTI-LEVEL QUALITY SPECIFICATIONS

Part	Quality Designators
Microelectronics	A, B, B-1, B-2, C
Discrete Semiconductors	JANTXV, JANTX, JAN
Capacitors, Established Reliability (ER)	L, M, P, R, S
Resistors, Established Reliability (ER)	M, P, R, S

Some parts are covered by older specifications, usually referred to as Non-ER, that do not have multi-levels of quality. These part models generally have three quality levels designated as "Upper", "Mil. Spec.", and "Lower". If the part is procured in complete accordance with the applicable specification, the π_Q value for Mil. Spec. should be used. If any requirements are waived or if a commercial part is procured the π_Q value for Lower should be used. The Upper quality level is provided because better than Mil. Spec. quality can be obtained; however, the use of the Upper π_Q should be treated with caution. The controls needed to produce this level vary from part to part and even within part sub-groups. The additional controls needed and the degree to which Mil. Spec. requirements should be tightened cannot be explicitly defined because of the wide part variety. Considerable engineering judgment is required and the use of Upper π_Q should be treated on an individual basis for each part. To aid in this determination, the following provides general guidance on the types of controls needed:

(1) Dust free assembly area continuously monitored and controlled.

(2) Tight production quality control from raw material state through acceptance, implemented by detailed written procedures, executed by personnel not reporting to production supervisor.

(3) Complete manufacturing drawing system with change procedures.

(4) Policy of assigning personnel with proven experience in producing parts of general type.

(5) Penalties imposed at working level for production of unreported defective assemblies (loss of incentive pay, etc.).

(6) Cleaning stations at major sub-assembly points.

(7) Flexible cleaning procedure to compensate for contaminant variations.

(8) Daily monitoring of contaminants.

(9) Mass spectrometer or Radiflo sealing inspection for hermetically sealed parts.

(10) Partial re-qualification testing procedure on maximum semi-monthly basis.

(11) Enforced procedure for maintenance of quality control records and for modifying production and inspection as needed including part failure analysis.

(12) Reliability screening.

The foregoing discussion involves the "as procured" part quality. Poor equipment design, production, and testing facilities can degrade part quality. The use of the higher quality parts requires a total equipment design and quality control process commensurate with the high part quality. It would make little sense to procure high quality parts only to have the equipment production procedures damage the parts or introduce latent defects. Total equipment program descriptions as they might vary with different part quality mixes is beyond the scope of this Handbook. Reliability management and quality control procedures are described in other DOD standards and publications. Nevertheless, when a proposed equipment development is pushing the state-of-the-art and has a high reliability requirement necessitating high quality parts, the total equipment program should be given careful scrutiny and not just the parts quality. Otherwise, the low failure rates as predicted by the models for high quality parts will not be valid.

c. Use Environment.

All part reliability models include the effects of environmental stresses through the factor, π_E. The definitions of these environments are shown in Table 2-3. The π_E factor is quantified within each part failure rate model. These environments encompass the major areas of equipment use. Some equipment may experience more than one environment during its normal use, e.g., equipment in spacecraft. In such a case, the reliability analysis should be segmented, namely, missile launch (M_L) conditions during boost and return from orbit, and space flight (S_F) while in orbit.

TABLE 2-3
ENVIRONMENTAL SYMBOL IDENTIFICATION AND DESCRIPTION

Environment	π_E Symbol	Nominal Environmental Conditions
Ground, Benign	G_B	Nearly zero environmental stress with optimum engineering operation and maintenance.
Space, Flight	S_F	Earth orbital. Approaches Ground, Benign conditions without access for maintenance. Vehicle neither under powered flight nor in atmospheric re-entry.
Ground, Fixed	G_F	Conditions less than ideal to include installation in permanent racks with adequate cooling air, maintenance by military personnel and possible installation in unheated buildings.
Ground, Mobile (and Portable)	G_M	Conditions more severe than those for G_F, mostly for vibration and shock. Cooling air supply may also be more limited, and maintenance less uniform.
Naval, Sheltered	N_S	Surface ship conditions similar to G_F but subject to occasional high shock and vibration.
Naval, Unsheltered	N_U	Nominal surface shipborne conditions but with repetitive high levels of shock and vibration.
Airborne, Inhabited	A_I	Typical cockpit conditions without environmental extremes of pressure, temperature, shock and vibration.
Airborne, Uninhabited	A_U	Bomb-bay, tail, or wing installations where extreme pressure, temperature, and vibration cycling may be aggravated by contamination from oil, hydraulic fluid, and engine exhaust. Classes I and Ia equipment of MIL-E-5400 should not be used in this environment.
Missile, Launch	M_L	Severe conditions of noise, vibration, and other environments related to missile launch, and space vehicle boost into orbit, vehicle re-entry and landing by parachute. Conditions may also apply to installation near main rocket engines during launch operations.

d. Part Failure Rate Models.

Part failure rate models for microelectronic parts are significantly different from those for other parts and are presented entirely in Section 2.1. Another type of model is used on most other parts; a typical example is the following one for discrete semiconductors:

$$\lambda_p = \lambda_b(\pi_E \times \pi_A \times \pi_{S2} \times \pi_C \times \pi_Q)$$

where λ_p is the part failure rate,

λ_b is the base failure rate usually expressed by a model relating the influence of electrical and temperature stresses on the part,

π_E and the other π factors modify the base failure rate for the category of environmental application and other parameters that affect the part reliability.

The π_E and π_Q factors are used in all models and other π factors apply only to specific models. The applicability of π factors is identified in each part subsection. An overall list of π factors used in models other than microelectronics is presented in Table 2-4.

The base failure rate (λ_b) models are presented in each part subsection along with identification of the applicable model factors. Tables of calculated λ_b values are also provided for use in manual calculations. The model equations can, of course, be incorporated into computer programs for machine processing. The tabulated values of λ_b are cut off at the part ratings with regard to temperature and stress, hence, use of parts beyond these cut off points will overstress the part. The use of the λ_b models in a computer program should take the part rating limits into account. The λ_b equations are mathematically continuous beyond the part ratings but such failure rate values are invalid in the over-stressed regions.

All the part models include both catastrophic and drift failures and are based upon a constant failure, except for some rotary devices that show an increasing failure rate. Failures associated with connection of parts into circuit assemblies are not included within the part failure rate models. Information on connection reliability is provided in Section 2.13.

e. Thermal Aspects.

The use of this prediction method requires the determination of the temperatures surrounding the parts. Since parts reliability is sensitive to temperature, the thermal analysis of any design should fairly accurately provide the ambient temperatures needed in using the part models. Of course, lower temperatures produce better reliability but also can produce increased penalties in terms of added loads on the environmental control system. The thermal analysis should be part of the design process and included in all the trade-off studies covering

TABLE 2-4

π FACTORS FOR PART FAILURE RATE MODELS EXCEPT MICROELECTRONICS

π Factor	Description
Common Factors - Used in all or many part categories.	
π_E	Environment - Accounts for influence of environmental factors other than temperature. Related to application categories (Table 2-3).
π_Q	Quality - accounts for effects of different quality levels.
Discrete Semiconductors	
π_A	Application - Accounts for effect of application in terms of circuit function.
π_C	Complexity - Accounts for effect of multiple devices in a single package.
π_{S2}	Voltage Stress - Adjusts model for a second electrical stress (application voltage) in addition to wattage included within λ_b.
Resistors	
π_R	Resistance - Adjusts model for the effect of resistor ohmic values.
π_C	Construction Class - Accounts for influence of construction class of variable resistors as defined in individual part specifications.
π_V	Voltage - Adjusts for effect of applied voltage in variable resistors in addition to wattage included within λ_b.
π_{TAPS}	Tap Connections on Potentiometers - Accounts for effect of multiple taps on resistance element.
Capacitors	
π_{SR}	Series Resistance - Adjusts model for the effect of series resistance in circuit application of some electrolytic capacitors.
π_{CV}	Capacitance Value - Adjusts model for effect of capacitance related to case size.
Inductive Devices	
π_F	Family - Adjusts model for influence of family type as defined by individual part specifications.

TABLE 2-4 (Cont.)

π FACTORS FOR PART FAILURE RATE MODELS EXCEPT MICROELECTRONICS

Rotating Devices	
π_F	Family - Accounts for motor family and commutator vs. brushless construction.
π_N	Windings - Accounts for number of windings.
Relays	
π_C	Contacts - Accounts for contact quantity and form.
π_{CYC}	Cycling - Accounts for time rate of actuation.
π_L	Load - Accounts for type of contact load.
π_F	Family - Accounts for construction and application.
Switches	
π_C	Contacts - Accounts for contact quantity and form.
π_{CYC}	Cycling - Accounts for time rate of actuation.
Connectors	
π_P	Contacts - Accounts for quantity of contacts.
λ_{CYC}	Cycling - Accounts for time rate of mating and unmating.

equipment performance, reliability, weight, volume, environmental control requirements, etc. For general guidance and detailed thermal analysis procedures, refer to "Reliability/Design Handbook, Thermal Applications", NAVELEX Publication No. 0967-437-7010, July 1973.

CAUTION

THE FAILURE RATES PRESENTED APPLY TO EQUIPMENT UNDER NORMAL OPERATING CONDITIONS, i.e., WITH POWER ON AND PERFORMING ITS INTENDED FUNCTIONS IN ITS INTENDED ENVIRONMENT. EXTRAPOLATION OF ANY OF THE BASE FAILURE RATE MODELS BEYOND THE TABULATED VALUES, SUCH AS HIGH OR SUB-ZERO TEMPERATURE, OR ELECTRICAL STRESS VALUES ABOVE 1.0 OR AT 0 OR EXTRAPOLATION OF ANY ASSOCIATED MODIFIERS IS COMPLETELY INVALID.

2.1 MICROELECTRONIC DEVICES.

This section presents failure rate prediction models for five major classes of microelectronic devices:

Monolithic Bipolar & MOS Digital (SSI/MSI)........Sect. 2.1.1
Monolithic Bipolar & MOS Linear ....Sect. 2.1.2
Monolithic Bipolar & MOS Digital (LSI)............Sect. 2.1.3
Monolithic Bipolar & MOS Memories.................Sect. 2.1.4
Hybrids...Sect. 2.1.7

In the title description of each monolithic device type, SSI, MSI, and LSI represent Small Scale Integration, Medium Scale Integration, and Large Scale Integration respectively, and indicate the complexity level for which the device model is applicable. MOS represents all metal-oxide semiconductor microcircuits which includes NMOS, PMOS, CMOS, and MNOS fabricated on various substrates, such as sapphire, polycrystalline, or single crystal silicon. From the I.C. chip standpoint, the hybrid model is structured to accommodate all of the monolithic chip types and the various complexity levels indicated.

Since different models are designated for the SSI/MSI and LSI Monolithic Digital devices, the following distinction in terms of complexity level is made in order to provide guidance in selection of the appropriate model. For the present, and until a new limit is established, devices having complexities less than 100 gates (approximately 400 transistors) are to be considered as SSI/MSI devices. More complex devices by gate count (or transistor count at 4 per gate) are to be considered as LSI devices. No distinction is made between SSI and MSI Monolithic Digital devices since the same model applies directly to both. Also, no distinction is made between the complexity factors for MOS and Bipolar devices in that the factors that define complexity are independent of the specific technologies.

For the purposes of this handbook, a gate is considered to be any one of the following logic functions: AND, OR, NAND, NOR, Exclusive OR, and Inverter. A J-K or R-S flip-flop is equivalent to 8 gates when used as part of a complex circuit. When the flip-flop is individually packaged (single, dual, or greater) the gate count should be determined from the schematic or logic diagram. For guidance in symbols used for these functions, see Standard ANSI Y32.14-1973, "Graphic Symbols for Logic Diagrams". This standard has been adopted by the Department of Defense and supersedes Mil-Std-806B (an earlier logic symbol standard).

Monolithic memories, because of their high gate-to-pin ratio, are not treated as a part of the SSI/MSI/LSI models. Their complexity factors are expressed in terms of the number of bits and are divided

into the two major categories of monolithic memories: random-access memories (RAMS), and read-only memories (ROMS). However, for the purposes of this handbook, programmable-read-only memories (PROMS) and content-addressable memories (CAMS) are considered in the same categories as ROMS and RAMS, respectively; therefore, the same models are applicable. For complex (larger than dual 8-bit) static and dynamic shift registers, use the RAM model with bit count. For smaller shift registers, use the Digital SSI/MSI model. For linear devices, both MOS and Bipolar, the same model expressing complexity in terms of the number of transistors is presented.

In order to help clarify some of the parameter descriptions for the various models, all of monolithic device models are based on a "$\lambda_T + \lambda_M$ additive model concept" - - i.e. $\lambda_P = \lambda_T + \lambda_M$, where:

λ_P is the overall device failure rate for monolithic devices.

λ_T is the failure rate component due to time degradation causes, and represents degradation mechanisms which are accelerated by temperature and electrical bias; composed largely of phenomena which follow the Arrhenius type rate acceleration.

λ_M is the failure rate component due to mechanical (application environment) causes, and represents failure mechanisms resulting from mechanical stresses directly, or indirectly (such as stresses set up by thermal expansion).

The monolithic device models, along with parameter descriptions and instructions for quantifying the parameters are presented in sections 2.1.1 through 2.1.4. The tables used for quantifying the model parameters are presented in section 2.1.5.

2.1.1 MONOLITHIC BIPOLAR AND MOS DIGITAL SSI/MSI DEVICES (less than 100 gates or 400 transistors).

$$\lambda_P = \pi_L \, \pi_Q \, (C_1 \, \pi_T + C_2 \, \pi_E)$$

where:

λ_P is the device failure rate in F./10^6 Hours

π_L is the device learning factor and its value is determined from Table 2.1.5-2.

π_Q is the quality factor, Table 2.1.5-1.

π_T is the temperature acceleration factor and its values, depending upon the device technology, are determined from Table 2.1.5-4.

π_E is the application environment multiplier and its values are determined from Table 2.1.5-3.

C_1, C_2 are the circuit complexity factors and are equal to:

C_1 = .00129 $(G)^{(0.67)}$

C_2 = .00389 $(G)^{(0.35)}$

where G is the number of gates (assume 4 transistors per gate). The C values are found in Table 2.1.5-5.

2.1.2 MONOLITHIC BIPOLAR AND MOS LINEAR DEVICES.

$$\lambda_P = \pi_L \pi_Q (C_1 \pi_{T2} + C_2 \pi_E)$$

where:

λ_P is the device failure rate in F./10^6 Hours

π_Q is quality factor, Table 2.1.5-1

π_L is the device learning factor and its value is determined from Table 2.1.5-2.

π_{T2} is the temperature acceleration factor and its values are determined from Figure 2.1.5-4.

π_E is the application environment multiplier and its values are determined from Table 2.1.5-3.

C_1, C_2 are the circuit complexity factors and are equal to:

$C_1 = .00056\ (T)^{0.76}$

$C_2 = .0026\ (T)^{0.55}$

where: T is the number of transistors. These C values are found in Table 2.1.5-6.

2.1.3 MONOLITHIC BIPOLAR AND MOS DIGITAL LSI DEVICES (equal to or greater than 100 gates or 400 transistors).

$$\lambda_P = \pi_L \pi_Q (C_1 \pi_T + C_2 \pi_E)$$

where:

λ_P is the device failure rate in F./10^6 Hours

π_L is the device learning factor and its value is determined from Table 2.1.5-2

π_T is the temperature acceleration factor and its values, depending upon the device technology, are found in Table 2.1.5—

π_Q is the quality factor, Table 2.1.5-1

π_E is the application environment multiplier and its values are determined from Table 2.1.5-3

C_1, C_2 are the circuit complexity factors and are equal to:

$$C_1 = .0187\ e^{(0.005G)}$$

$$C_2 = .013\ e^{(0.004G)}$$

Where: G is the number of gates (assume 4 transistors per gate) and e is the natural logarithm base, 2.718. The C values are found in Table 2.1.5-7.

2.1.4 MONOLITHIC MOS AND BIPOLAR MEMORIES.

$$\lambda_P = \pi_L \pi_Q (C_1 \pi_T + C_2 \pi_E)$$

where: λ_P is the device failure rate in F./10^6 hours

π_L is the device learning factor and its value is determined from Table 2.1.5-2.

π_Q is the quality factor, Table 2.1.5-1.

π_T is the temperature acceleration factor and its values, depending upon the device technology, are determined from Table 2.1.5-4.

π_E is the application environment multiplier and its values are determined from Table 2.1.5-3.

C_1, C_2 are the circuit complexity factors and are:

For RAMS

$$C_1 = .00199 \, B^{(0.603)}$$

$$C_2 = .00056 \, B^{(0.644)}$$

For ROMS

$$C_1 = .00114 \, B^{(0.603)}$$

$$C_2 = .00032 \, B^{(0.646)}$$

Where B is the number of bits. These C values are found in Table 2.1.5-8.

2.1.5 FIGURES AND TABLES FOR THE MONOLITHIC MODEL PARAMETERS

This section presents the tables and figures for quantifying the parameters of the failure rate models in sections 2.1.1 through 2.1.4 for the various monolithic microelectronic device types. The tables are presented first, and then the figures.

TABLE 2.1.5-1

π_Q, QUALITY FACTORS

Quality Level or Screen Class	Description	π_Q
A	Mil-M-38510, Class A (JAN)	1
B	Mil-M-38510, Class B (JAN)	2
B-1	Mil-Std-883, Method 5004, Class B	5
B-2	Vendor Equivalent of Mil-Std-883, Method 5004, Class B	10
C	Mil-M-38510, Class C (JAN)	16
D	Commercial (or non-mil standard) part, with no screening beyond the manufacturer's regular quality assurance practices. The indicated π_Q value represents an average for all grades of commercial parts.	150

TABLE 2.1.5-2

π_L, LEARNING FACTORS

The learning factor π_L is 10 under any of the following conditions:

(1) New device in initial production.
(2) Where major changes in design or process have occurred.
(3) Where there has been an extended interruption in production or a change in line personnel (radical expansion).

The factor of 10 can be expected to apply until conditions and controls have stabilized. This period can extend for as much as six months of continuous production.

π_L is equal to 1.0 under all production conditions not stated in (1), (2) and (3) above.

TABLE 2.1.5-3

APPLICATION ENVIRONMENT FACTOR, π_E

Application Environment	Symbol	π_E
Ground, Benign	G_B	0.2
Space Flight	S_F	0.2
Ground, Fixed	G_F	1.0
Airborne, Inhabited	A_I	4.0
Naval, Sheltered	N_S	4.0
Ground, Mobile	G_M	4.0
Airborne, Uninhabited	A_U	6.0
Naval, Unsheltered	N_U	5.0
Satellite or Missile Launch	M_L	10.0

TABLE 2.1.5-4
π_T vs. JUNCTION TEMPERATURE (See Notes below)

T_j (°C.)	π_{T1}	π_{T2}	T_j (°C.)	π_{T1}	π_{T2}	T_j (°C.)	π_{T1}	π_{T2}	T_j (°C.)	π_{T1}	π_{T2}
25	.10	.10	51	.36	.89	77	1.1	5.7	103	2.8	28.
27	.11	.12	53	.40	1.0	79	1.2	6.5	105	3.0	32.
29	.12	.14	55	.44	1.2	81	1.3	7.5	110	3.6	42.
31	.14	.17	57	.48	1.4	83	1.4	8.5	115	4.2	56.
33	.15	.20	59	.52	1.6	85	1.5	9.6	120	4.9	73.
35	.17	.24	61	.57	1.9	87	1.6	11.	125	5.7	94.
37	.19	.29	63	.62	2.2	89	1.7	12.	135	7.7	155.
39	.21	.34	65	.67	2.5	91	1.9	14.	145	10.	250.
41	.23	.40	67	.73	2.9	93	2.0	16.	155	13.	390.
43	.25	.47	69	.79	3.3	95	2.1	18.	165	17.	610.
45	.28	.56	71	.86	3.8	97	2.3	20.	175	22.	920.
47	.30	.65	73	.93	4.4	99	2.5	23.			
49	.33	.76	75	1.0	5.0	101	2.6	25.			

NOTES:

1. π_{T1} is applicable to Bipolar digital devices, i.e., TTL & DTL, not included in Note 2 below.

$$\pi_{T1} = 0.1e^{X}$$

$$\text{where: } x = -4794\left(\frac{1}{T_j+273} - \frac{1}{298}\right)$$

2. π_{T2} is applicable to Bipolar & MOS Linear, Bipolar Beam Lead, Bipolar ECL, and all other MOS devices.

$$\pi_{T2} = 0.1\,e^{x}$$

$$\text{where } x = -8121\left(\frac{1}{T_j + 273} - \frac{1}{298}\right)$$

3. In Notes 1 & 2 above, T_j is worst case junction temperature (°C.) and e is natural logarithm base, 2.718.

If T_j is unknown, use following approximations:

For packaged monolithic devices use

T_j = ambient T + 10°C. if no. of transistors $\leq$ 120.

T_j = ambient T + 25°C. if no. of transistors > 120.

TABLE 2.1.5-5

C_1 & C_2, COMPLEXITY FACTORS FOR SSI/MSI DEVICES (See Notes below)

No. GATES	C_1	C_2	No. GATES	C_1	C_2	No. GATES	C_1	C_2	No. GATES	C_1	C_2
1	.0013	.0039	24	.011	.012	48	.018	.016	72	.023	.018
2	.0021	.0050	26	.012	.013	50	.018	.016	74	.024	.018
4	.0033	.0064	28	.012	.013	52	.019	.016	76	.024	.019
6	.0043	.0074	30	.013	.013	54	.019	.016	78	.025	.019
8	.0053	.0082	32	.014	.014	56	.020	.017	80	.025	.019
10	.0061	.0089	34	.014	.014	58	.020	.017	85	.026	.019
12	.0069	.0095	36	.015	.014	60	.021	.017	90	.027	.020
14	.0077	.010	38	.015	.014	62	.021	.017	95	.028	.020
16	.0084	.011	40	.016	.015	64	.022	.017	99	.029	.020
18	.0091	.011	42	.016	.015	66	.022	.018			
20	.0098	.011	44	.017	.015	68	.022	.018			
22	.011	.012	46	.017	.015	70	.023	.018			

NOTES:

1. Tabulated values are derived from the following equations:

$$C_1 = 1.29(10)^{-3}(N_G)^{0.677} \quad C_2 = 3.89(10)^{-3}(N_G)^{0.359}$$

where N_G = no. of gates (assume 4 transistors/gate).

2. The tabulated values are applicable to devices in packages containing up to 22 pins. For larger packages multiply the values by:

No. of Pins	Multiplier
24 to 40	1.1
42 to 64	1.2
>64	1.3

TABLE 2.1.5-6

C_1 & C_2, COMPLEXITY FACTORS FOR LINEAR DEVICES (See Note below)

No. of Transistors	C_1	C_2	No. of Transistors	C_1	C_2	No. of Transistors	C_1	C_2
4	.0016	.0056	64	.014	.025	148	.025	.040
8	.0027	.0081	68	.014	.026	156	.026	.041
12	.0037	.010	72	.015	.027	164	.027	.043
16	.0046	.012	76	.015	.028	172	.028	.044
20	.0055	.013	80	.016	.029	180	.029	.045
24	.0063	.015	84	.016	.030	188	.030	.046
28	.0071	.016	88	.017	.030	196	.031	.047
32	.0079	.017	92	.018	.031	204	.032	.048
36	.0086	.019	96	.018	.032	220	.034	.050
40	.0093	.020	100	.019	.032	236	.036	.052
44	.010	.021	108	.020	.034	252	.038	.054
48	.011	.022	116	.020	.035	268	.040	.056
52	.011	.023	124	.022	.036	284	.042	.057
56	.012	.024	132	.023	.038	300	.043	.059
60	.013	.025	140	.024	.039			

NOTE:

The tabulated values are derived from the following equations:

$C_1 = .00056\ (N_T)^{0.763}$ $\qquad$ $C_2 = .0026\ (N_T)^{0.547}$

where: N_T = no. of transistors.

TABLE 2.1.5-7
C_1 & C_2, COMPLEXITY FACTORS FOR LSI DEVICES (See Notes below)

No. GATES	C_1	C_2	No. GATES	C_1	C_2	No. GATES	C_1	C_2	No. GATES	C_1	C_2
100	.030	.020	330	.088	.053	610	.33	.17	890	1.2	.56
110	.031	.021	350	.097	.057	630	.36	.19	910	1.4	.62
120	.033	.022	370	.11	.062	650	.40	.20	930	1.5	.67
130	.034	.023	390	.12	.068	670	.44	.22	950	1.6	.73
140	.036	.024	410	.13	.074	690	.48	.24	970	1.8	.79
150	.038	.025	430	.14	.080	710	.53	.26	990	2.0	.86
170	.042	.028	450	.16	.088	730	.58	.29	1010	2.2	.94
190	.046	.029	470	.17	.095	750	.64	.31	1050	2.6	1.1
210	.050	.032	490	.19	.10	770	.70	.34	1100	3.3	1.4
230	.055	.034	510	.21	.11	790	.77	.37	1150	4.2	1.7
250	.061	.038	530	.23	.12	810	.85	.40	1200	5.3	2.1
270	.067	.041	550	.25	.13	830	.93	.44	1250	6.7	2.6
290	.073	.044	570	.27	.15	850	1.0	.48	1300	8.5	3.2
310	.080	.048	590	.30	.16	870	1.1	.52			

NOTES:

1. Tabulated values are derived from the following equations:

   $C_1 = .0187\ e^{(.00471)N_G}$ $\qquad C_2 = .013\ e^{(.00423)\ N_G}$

   where N_G = no. of gates (assume 4 transistors/gate)

   and e = natural logarithm base, 2.718.

2. The tabulated values are applicable to devices in packages containing up to 24 pins. For larger packages, multiply values by:

No. of Pins	Multiplier
26 to 64	1.1
>64	1.2

TABLE 2.1.5-8
C_1 & C_2, COMPLEXITY FACTORS FOR MEMORIES (See Notes below)

No. of BITS	ROMS		RAMS	
	C_1	C_2	C_1	C_2
16	.0061	.0019	.011	.0033
32	.0092	.0030	.016	.0052
64	.014	.0047	.025	.0081
128	.021	.0074	.037	.013
256	.032	.012	.056	.020
320	.037	.013	.065	.023
512	.049	.018	.086	.031
576	.053	.020	.092	.034
1024	.074	.028	.13	.049
1120	.078	.030	.14	.052
1280	.085	.033	.15	.056
2048	.11	.044	.20	.076
2240	.12	.047	.21	.081
2560	.13	.051	.23	.088
4096	.17	.070	.30	.12
8192	.26	.11	.46	.19
9216	.28	.12	.49	.20
10240	.30	.13	.52	.22
12288	.33	.14	.58	.24
14848	.37	.16	.65	.27
16384	.40	.17	.69	.29

NOTES:

1. Tabulated values are derived from the following equations:

For ROMS - $C_1 = .00114(B)^{0.603}$ $\quad C_2 = .00032(B)^{0.646}$

For RAMS - $C_1 = .00199(B)^{0.603}$ $\quad C_2 = .00056(B)^{0.644}$

where: B = number of bits.

2. The tabulated values are applicable to devices in packages containing up to 24 pins. For packages with greater than 24 pins, multiply tabulated value by 1.1.

APPENDIX B (TO TR 2020 APPENDIX F):
EXCERPTS FROM RCA WARRANTIES

IVM-2
8/30/76

TERMS AND CONDITIONS OF SALE

Applicable to the Sale of Closed Circuit Video Equipment such as Television Cameras, Monitors, and Accessories.

7. OTHER WARRANTIES

(a) RCA warrants its products against defects in material or workmanship for the periods specified in the adjustment terms set forth on the applicable Price Schedule. (b) Said warranty does not apply if product malfunction is the result of misuse, abuse, improper installation or application, alteration, accident, or negligence in use, storage, transportation or handling, or if the original identification markings on the product have been removed, defaced or altered. (c) In order to permit RCA to properly administer this warranty, the Customer shall i) notify RCA promptly in writing of any claims, and ii) provide RCA with the opportunity to inspect and test the product claimed to be defective. Such inspection may be on the Customer's premises and/or RCA may request the return of the product, transportation charges prepaid, for more thorough examination. However, RCA cannot be responsible for packing, inspection, or labor costs in connection with the return of product. In order to avoid administrative difficulties that result from unauthorized returns, the Customer shall request a formal Return Authorization from RCA before returning product for any reason. (d) The liability of RCA hereunder is solely and exclusively limited to replacement, repair or credit at the price on the date of claim at RCA's option, for any product which is returned by the Customer during the applicable warranty period and which is found by RCA to be subject to adjustment under this warranty. In no event shall RCA be liable for special, indirect, incidental or consequential damages whether in contract, tort or negligence. (e) This warranty extends only to Customers of RCA and not to purchasers or users of said Customer's products.

RCA MAKES NO OTHER OR FURTHER WARRANTY, EXPRESS OR IMPLIED, INCLUDING ANY WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE OR WARRANTY OF MERCHANTABILITY.

It is recognized that some purchasers of the TC1150 and TC1155 may wish to evaluate the state-of-the-art technology of RCA SIDs, and some may even wish to explore alternate operating modes. A complete schematic drawing and functional block diagram has been shipped with your camera which, when taken in conjunction with the camera data sheet and the SID51232 sensor data sheet, should facilitate a more complete understanding of this new method of television image sensing. HOWEVER, IT SHOULD BE NOTED THAT RCA CANNOT BE RESPONSIBLE FOR ANY CAMERA WHICH HAS BEEN TAMPERED WITH INTERNALLY OR MODIFIED IN ANY WAY.

LIMITED WARRANTY*

RCA warrants the camera when purchased new to be free from defects in material and workmanship and will repair or replace, at RCA's option, any camera which under the proper conditions of installation and use exhibits such defects, provided that the product is returned properly packed, transportation prepaid under the proper Return Authorization paperwork (obtained from your local RCA Technical Sales Representative) to: RCA Camera Repair Center, New Holland Avenue, Lancaster, Pa. 17604.

Full adjustment will be made for the camera or any part thereof (including the SID51232 sensor) found to be defective upon inspection or test, provided that the claim is made within 90 days from the date of shipment from RCA.

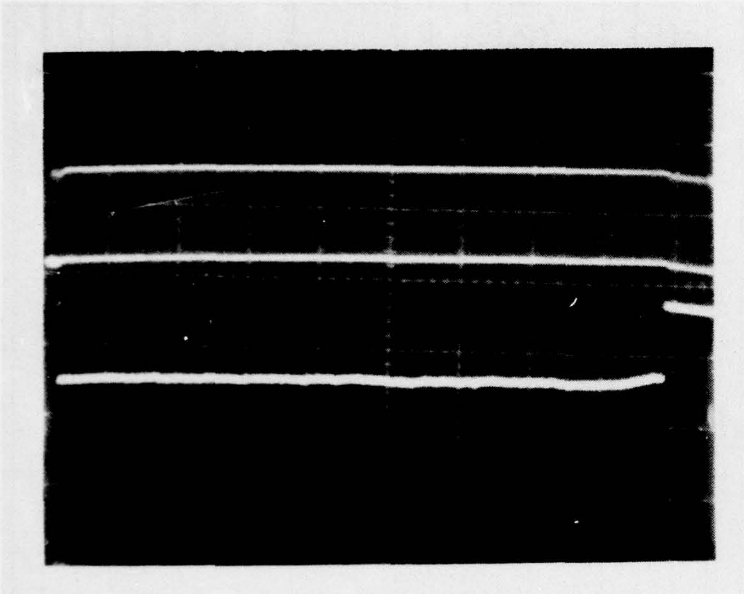
In no event shall RCA be liable for special, indirect, incidental or consequential damages, the original user's remedies being limited to repair or replacement.

RCA MAKES NO OTHER OR FURTHER WARRANTY, EXPRESS OR IMPLIED, INCLUDING ANY WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE OR WARRANTY OF MERCHANTABILITY.

CCD121
1728–ELEMENT LINEAR IMAGE SENSOR
CHARGE COUPLED DEVICE

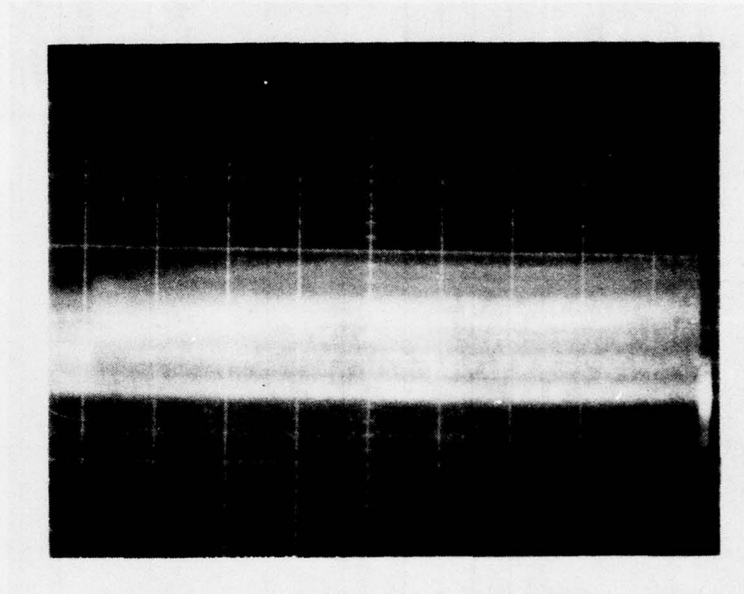
SERIAL # 435177 10A C27 12 SECOND UNIT

LINEAR OPERATION
50% SATURATION



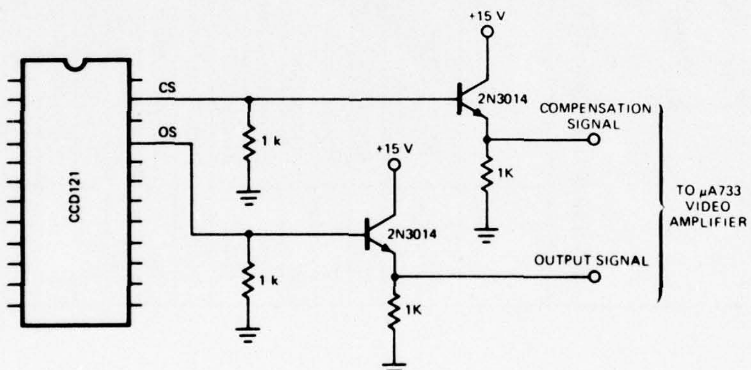
1.0v/ Div.

DARK SIGNAL OUTPUT



.05v/ Div.

TEST LOAD CONFIGURATION



CLOCK CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	RANGE MIN	TYP	MAX	UNITS	CONDITIONS
$V_{\phi 1AL}$, $V_{\phi 1BL}$ $V_{\phi 2AL}$, $V_{\phi 2BL}$	Analog Shift Register Transport Clocks LOW	0.0	0.5	0.8	V	Notes 3, 4
$V_{\phi 1AH}$, $V_{\phi 1BH}$ $V_{\phi 2AH}$ $\phi 2BH$	Analog Shift Register Transport Clocks HIGH		7			Notes 3, 4, 12
$V_{\phi XAL}$	Transfer Gate Clock LOW	0.0	0.5	0.8	V	Notes 3,4
$V_{\phi XAH}$	Transfer Gate Clock HIGH		7		V	Notes 3, 4, 12
$V_{\phi RL}$	Reset Clock Low	0.0	0.5	0.8	V	Notes 3, 4
$V_{\phi RH}$	Reset Clock HIGH		10			
$f_{\phi 1A}$, $f_{\phi 1B}$ $f_{\phi 2A}$, $f_{\phi 2B}$	Analog Shift Register Transport Clock Frequency		0.5		MHz	Notes 5, 6
$f_{\phi R}$	Reset Clock Frequency (Output Bit Rate)		1.0		MHz	Notes 5, 6

AC CHARACTERISTICS: T_A = 25°C, $f_{\phi 1} = f_{\phi 2}$ = 0.5 MHz, $f_{\phi R}$ = 1 MHz, $t_{INT} \cong$ 1.94 ms, $t_{TRANSFER}$ = 1.73 ms

SYMBOL	PARAMETER	RANGE MIN	TYP	MAX	UNITS	CONDITIONS
DR	Dynamic Range		500			Notes, 7, 8, 9
NEE	Peak-to-Peak Equivalent Exposure		1×10^{-3}		$\mu J/cm^2$	Notes 8, 9
SE	Saturation Exposure		0.5		$\mu J/cm^2$	Notes 8, 9
SR	Spectral Response Range Limits	0.45		1.05	μm	
R	Responsivity		0.4		V per $\mu J/cm^2$	Note 13
PRNU	Photoresponse Non-uniformity		±2.1	±10	T of V_{sat}	Note 10
ADS	Average Dark Signal		1.4		% of V_{sat}	
DSNU	Dark Signal Non-uniformity		2.8		% of V_{sat}	
V_{sat}	Saturation Output Voltage	100	140		mV	Note 11
P	Power Dissipation		100		mW	V_{OD} = 15 V
Z	Output Impedance		1000		Ω	
N	Peak-to-Peak Noise		400		μV	
RSO	Rate of Average Signal Offset		1		mV/ms	

DC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	RANGE MIN	TYP	MAX	UNITS	CONDITIONS
V_{OD}	Output Transistor Drain Voltage	14.5	15.0	15.5	V	
V_{RD}	Reset Transistor Drain Voltage	14.5	15.0	15.5	V	
V_{OG}	Output Gate Voltage		5			Note 1
V_{PG}	Photogate Voltage		8		V	Note 2
TP1 TP3	Test Points		0.0		V	
TP2 TP4	Test Points	14.5	15.0	15.5	V	